

# HM42-CP Block Diagram

PCB P/N : 48.4GW01.011  
REVISION : -1 09920

Project code: 91.4GW01.001 (HM42-CP)  
91.4GY01.001 (JE40-CP)  
91.4GZ01.001 (SJV41-CP)  
91.4JD01.001 (BA40-CP)

Clock Generator  
ICS9LRS3197AKLFT

X2  
14.318Mhz

DDRIII Slot 0  
800/1066

DDRIII Slot 1  
800/1066

DDRII Channel A

DDR II Channel B

Intel CPU  
Arrandale

4, 5, ..., 9, 10

FDI x8

DMI x4

X3  
27Mhz

N11P-GE1  
N11M-GE1  
Nvida

RGB CRT

LVDS 1CH

HDMI

CRT

LCD  
WXGA+

HDMI

SYSTEM DC/DC  
RT8223

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC  
RT8209E

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC  
RT8209E

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 1D05V_S0

SYSTEM DC/DC  
RT9025

INPUTS	OUTPUTS
DCBATOUT	1D8V_S0

SYSTEM DC/DC  
RT8209E

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

SYSTEM DC/DC  
TPS5161

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

CPU DC/DC  
ISL62882C

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

CHARGER  
ISL88731C

INPUTS	OUTPUTS
DCBATOUT	BT+

Discrete N11M

緯創資通

Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Block Diagram

Size

Document Number

HM42-CP

Rev

SC

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Mini-Card  
WLAN

Mini-Card  
3G

PCIE

USB 2.0

RJ45  
CONN

Giga LAN  
BCM57780

PCIE

X1  
25Mhz

X5  
25Mhz

MIC IN

INT MIC

HD AUDIO  
CODEC  
ALC272

AZALIA

PCB STACKUP

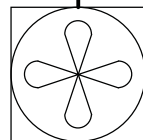
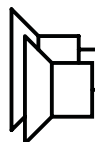
TOP  
GND  
S  
S  
GND  
BOTTOM

LINE OUT

2CH SPEAKER

OP AMP  
G1454

34



CPU FAN

INTEL  
PCH  
14 USB 2.0/1.1 ports  
ETHERNET (10/100/1000Mb)  
High Definition Audio  
6 SATA ports  
8 PCIE ports  
ACPI 1.1  
LPC I/F  
PCI/PCI BRIDGE

11, 12, ..., 18, 19

X6  
32.768Khz

LPC Bus

LPC debug

X4  
32.768Khz

KBC  
ENE 3930

SPI

Flash ROM  
128KB

Thermal  
Sensor

G792

Touch  
PAD

Int.  
KB

Card Reader  
AU 6433

37

SD/MMC  
MS/MS Pro/xD

37

SATA HDD

26

SATA ODD

27

Flash ROM  
4MB

41

BA40\_Power\_BD  
09768-1

A B C D E

# PCH Strapping

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> <b>Default Mode:</b> Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	<b>Default Mode:</b> Internal pull-up. <b>Low (0) = Top Block Swap Mode</b> (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	<b>High (1) = Integrated VRM is enabled</b> <b>Low (0) = Integrated VRM is disabled</b>
GNT0#, GNT1#	<b>Default (SPI):</b> Left both GNT0# and GNT1# floating. No pull up required. <b>Boot from PCI:</b> Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. <b>Boot from LPC:</b> Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	<b>Default - Internal pull-up.</b> <b>Low (0)=</b> Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	<b>Default:</b> Do not pull low. <b>Disable ME in Manufacturing Mode:</b> Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	<b>Enable iTPM:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable iTPM:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Danbury:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable Danbury:</b> Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	<b>Low (0):</b> Flash Descriptor Security will be overridden. <b>High (1) :</b> Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	<b>Default = Do not connect (floating)</b> High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

# Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	<b>Embedded DisplayPort Presence</b>	<b>1:</b> Disabled - No Physical Display Port attached to Embedded DisplayPort. <b>0:</b> Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	<b>PCI-Express Static Lane Reversal</b>	<b>1:</b> Normal Operation. <b>0:</b> Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	<b>PCI-Express Configuration Select</b>	<b>1:</b> Single PCI-Express Graphics <b>0:</b> Bifurcation enabled	1
CFG[7]	<b>Reserved - Temporarily used for early Clarksfield samples.</b>	<b>Clarksfield (only for early samples pre-ES1) -</b> Connect to GND with 3.01K Ohm/5% resistor <b>Note:</b> Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

## USB Table

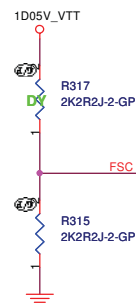
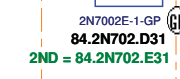
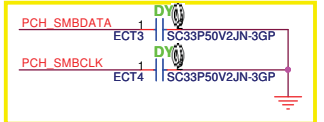
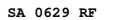
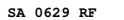
## PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

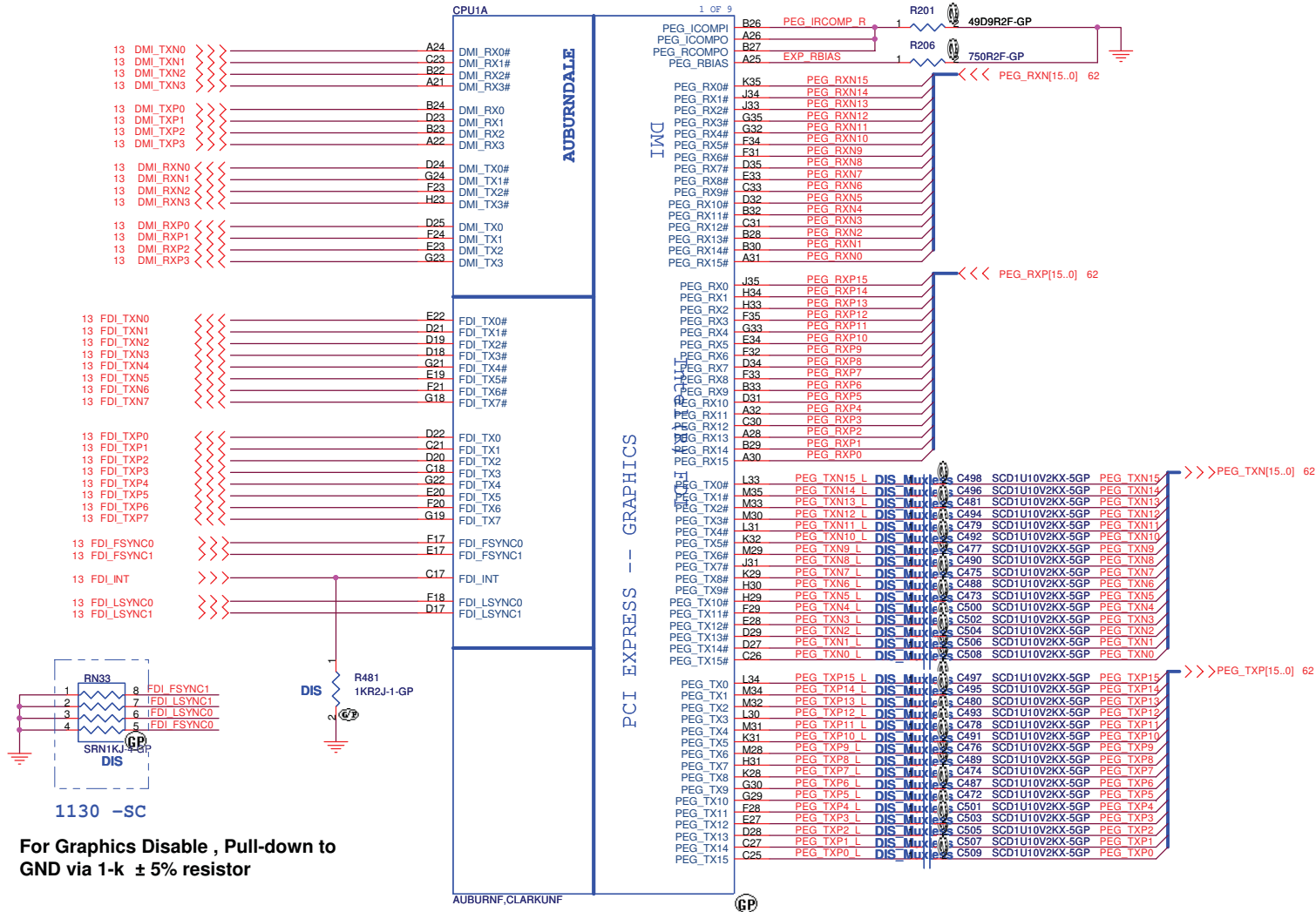
Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1 (HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

<Variant Name>

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SB 0813  $\frac{CL}{Freq} = 10pF$  tolerance : +/- 30 ppm



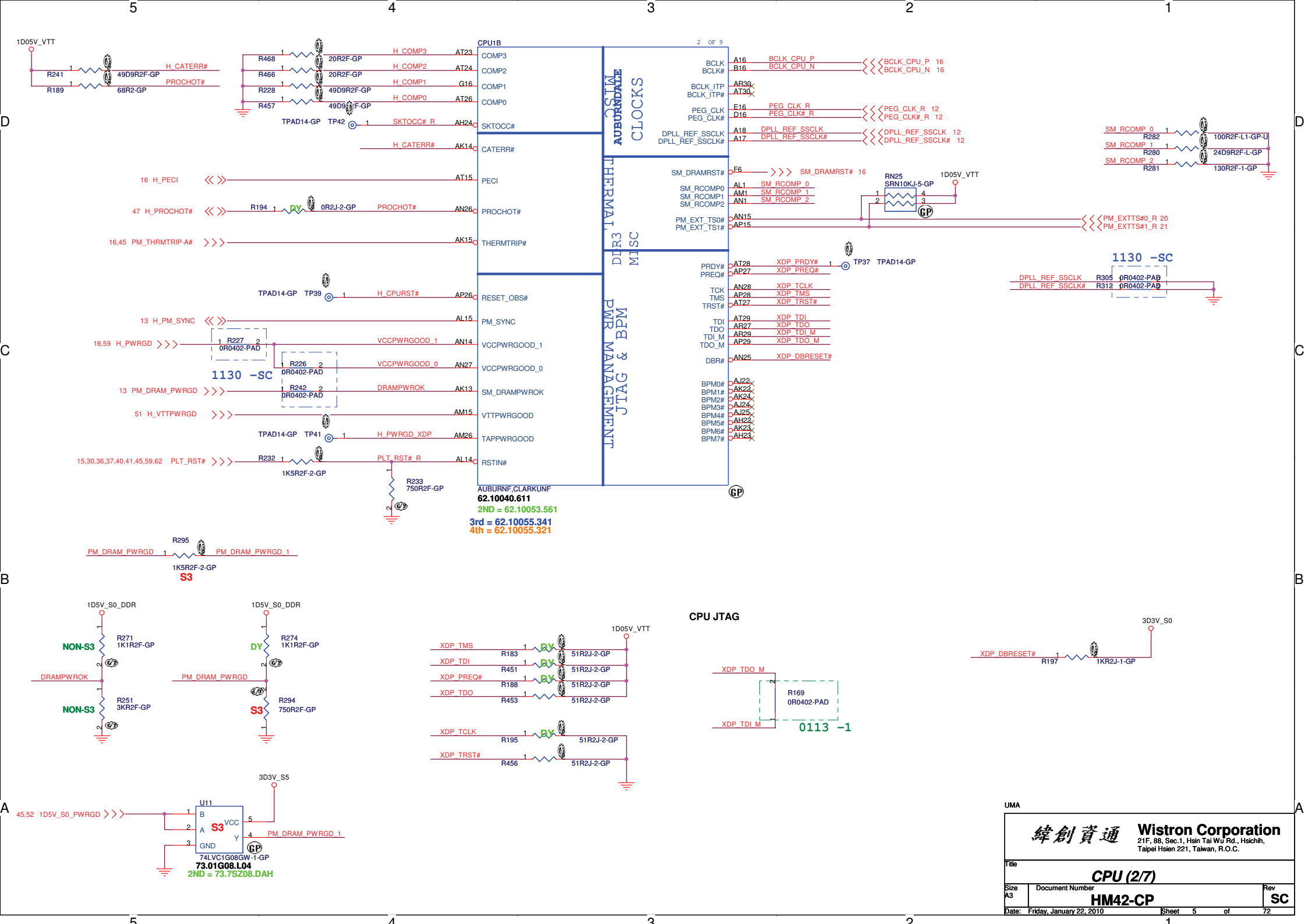
0113 -1

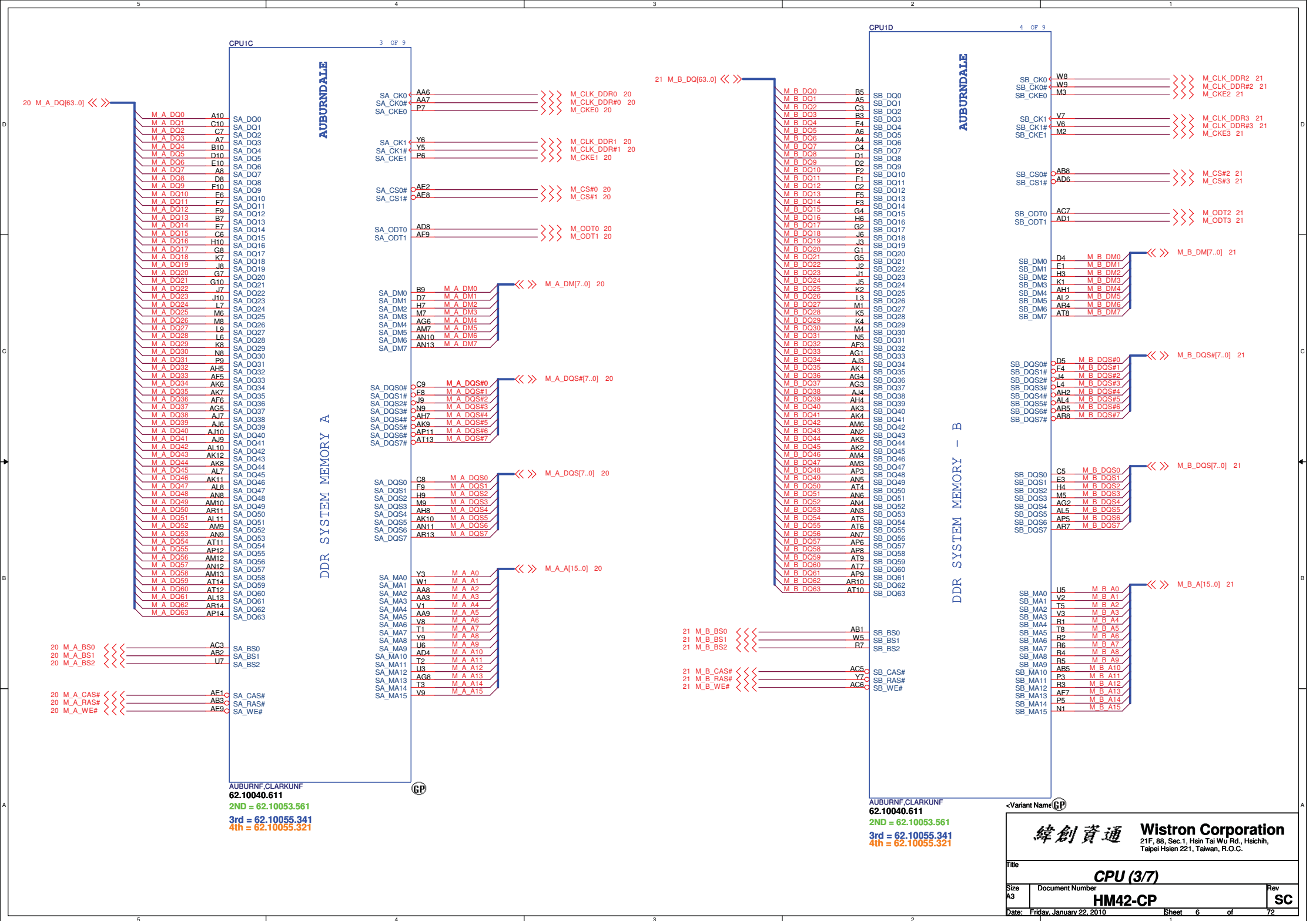
62.10040.611  
 2ND = 62.10055.341  
 3RD = 62.10055.341  
 4th = 62.10055.321

pel 3rd 62.10055.341 and 4th 62.10055.321  
 3rd and 4th have been purged  
 CE will confirm SQM if it can add BOM  
 CE will release EC to add to BOM

lab stuff 2nd,3rd and 4 th in BOM  
 Eng add 1st source(62.10040.611)  
 Eng do not stuff 4 th in BOM  
 because 4 th have been purge ,so stuff 1st in BOM  
 but CE said, 4th need stuff in PD if not any concern

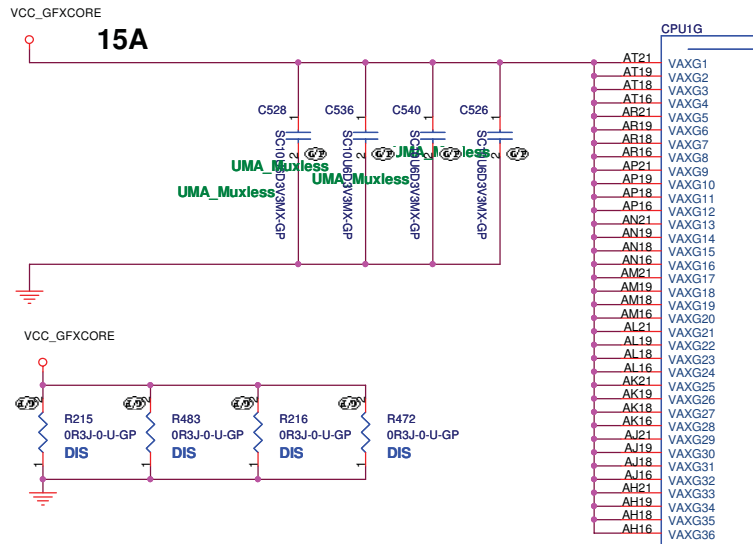
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 Taipei Hsien 221, Taiwan, R.O.C.



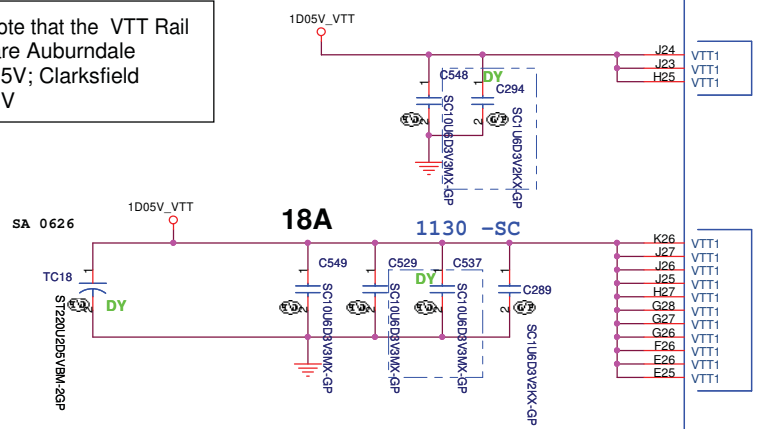






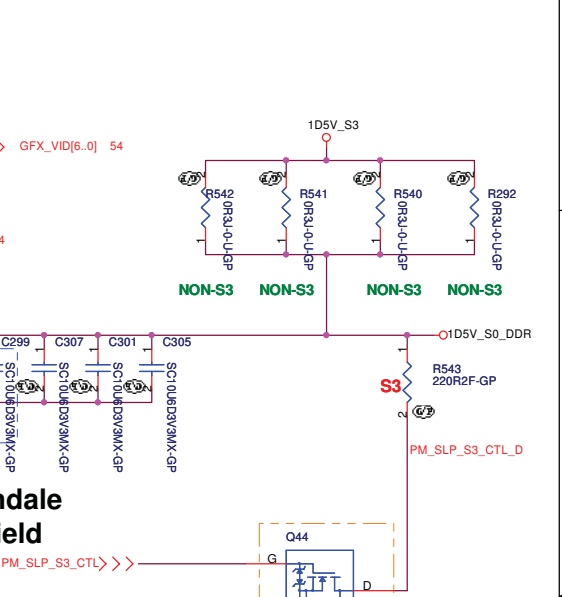
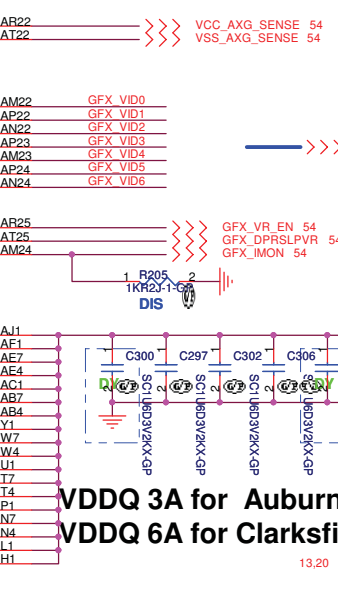
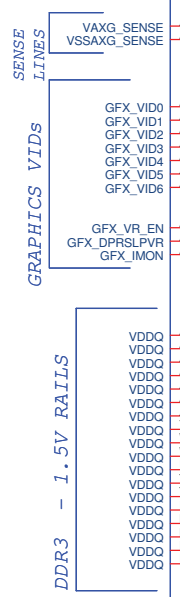


Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

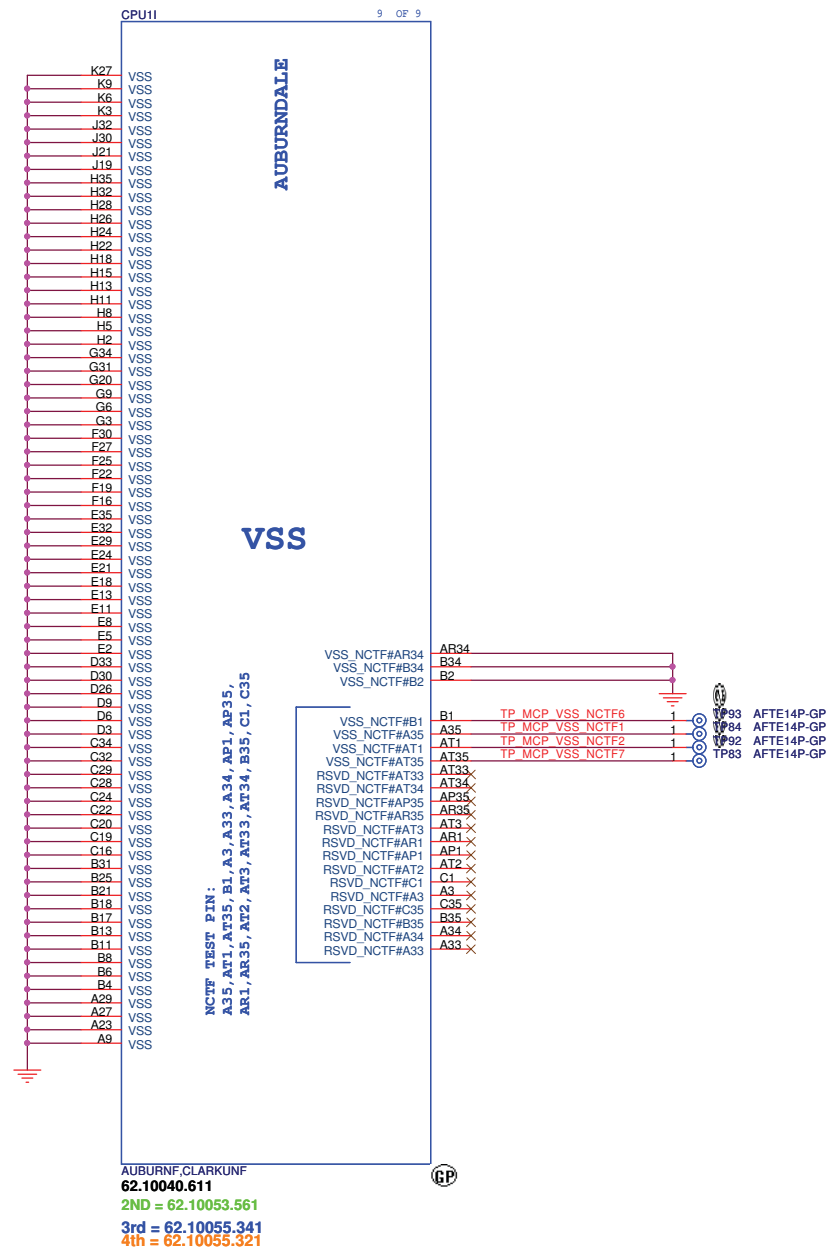
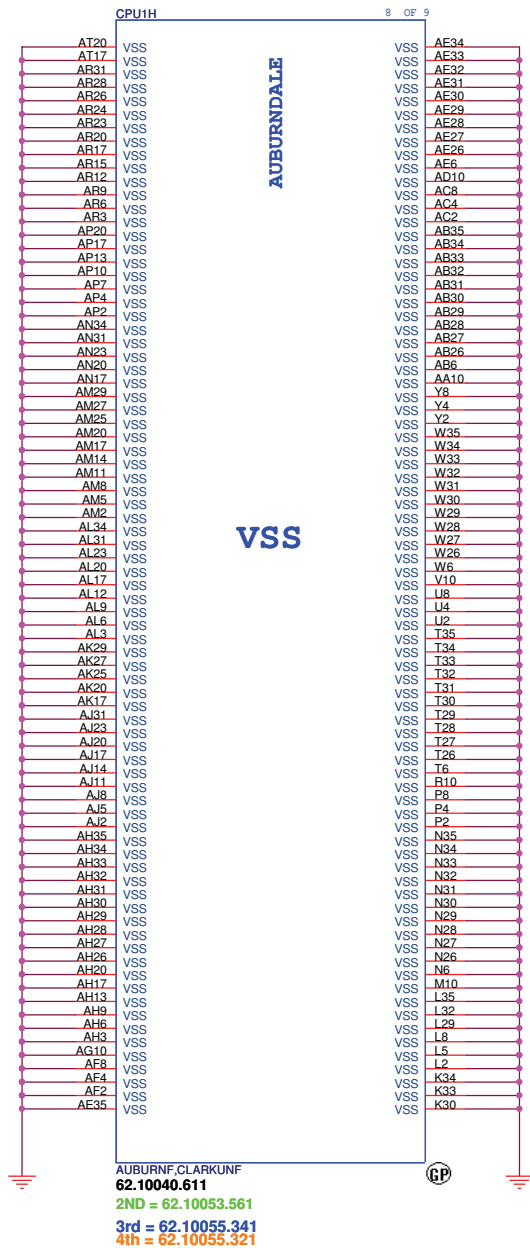


AUBURN, CLARKUNF  
62.10040.611  
2ND = 62.10053.561  
3rd = 62.10055.341  
4th = 62.10055.321

# **AUBURDALE** **GRAPHICS** **POWER** **PEG & DMI**



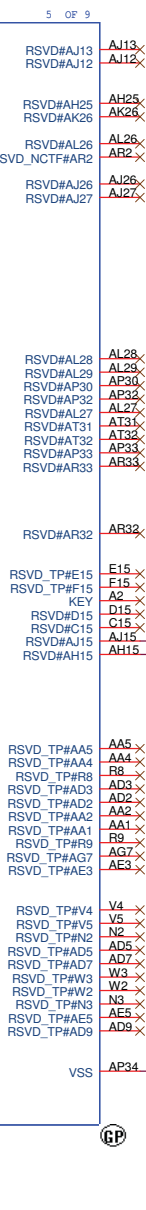
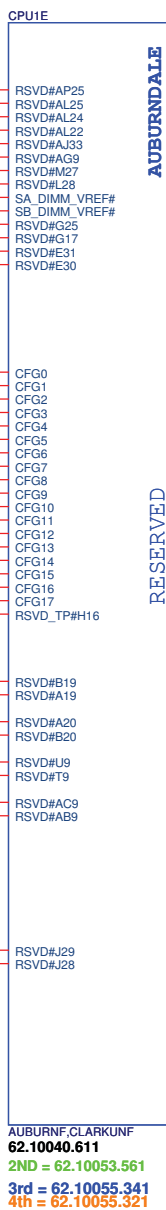
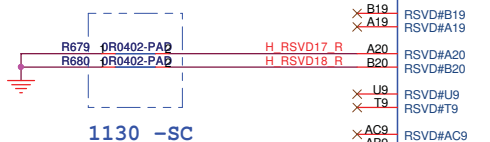
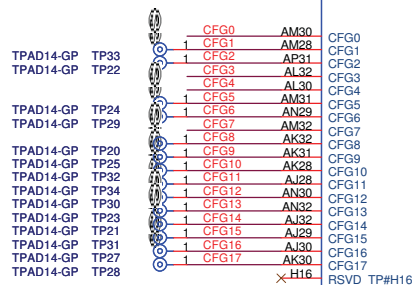
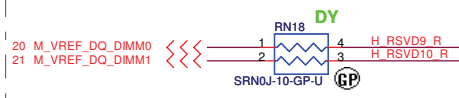




<Variant Name>

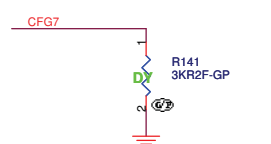
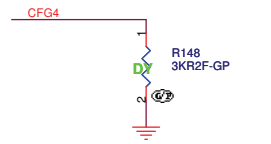
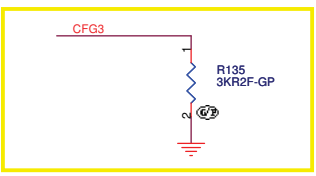
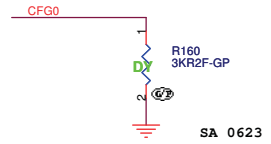
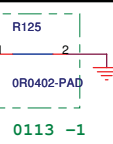
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Title		
CPU (6/7)		
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## SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor



1130 -SC

VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



## Processor Strapping

PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled

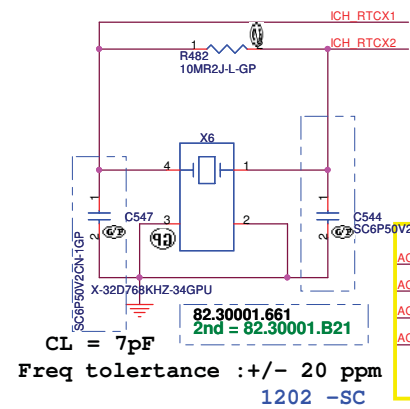
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation(Default) 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0:Enabled; An external Display Port device is connected to the Embedded Display Port

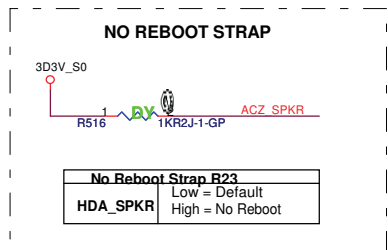
CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.  Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

<Variant Name>

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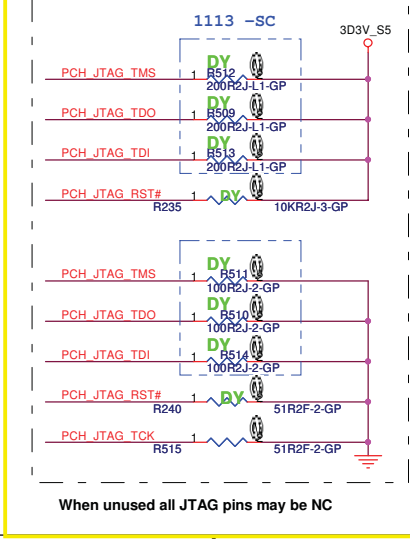


1117 -SC  
SIV fail when stuff 10-ohm,  
fine tune 33-ohm for solving  
33-ohm is required for intel recommend,  
real value base on fine tune result

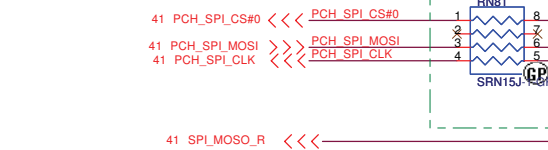


SA 0709

For after PCH stepping B3, have to DY,

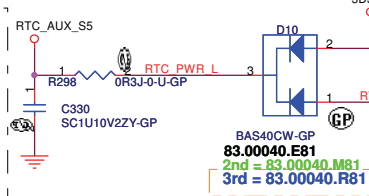
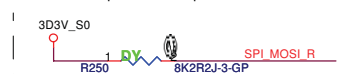


SPI\_CS0#, SPI\_MISO, SPI\_MOSI, SPI\_CLK:  
No series resistor required if routing length is 1.5"-6.5"



## PCH Strapping

**SPI\_MOSI** Enable iTPM: Connect to Vcc3\_3 with 8.2-kΩ weak pull-up resistor.  
Disable iTPM: Left floating, no pull-down required

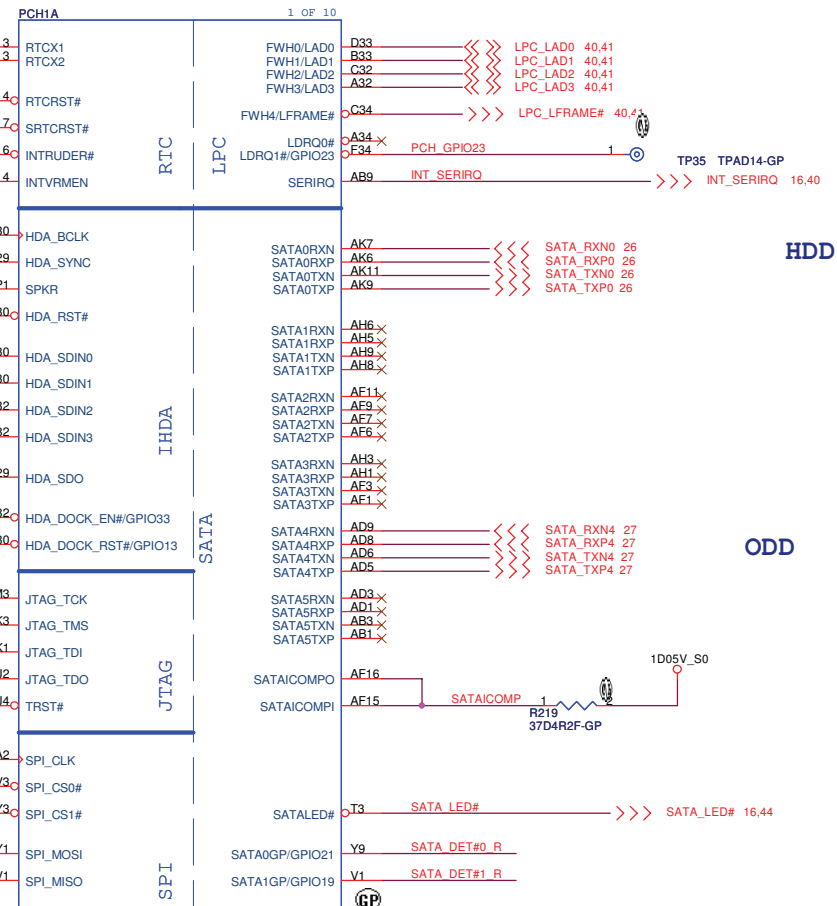


83.00040.Q81 is ROHS parts  
83.00040.R81 is Halogens free Part  
arrange qual in Eng SKU

1130 -SC  
0113 -1

INTVRMEN- Integrated SUS  
1.1V VRM Enable  
High - Enable internal VRs

Integrated VccSusi_05, VccSusi1_5, VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable



PCH 1 stuff 71.0IBEX.G0U

20.F1035.002  
2nd = 20.F0772.002  
3rd = 21.D0300.102  
4th = 20.F1729.002

UMA

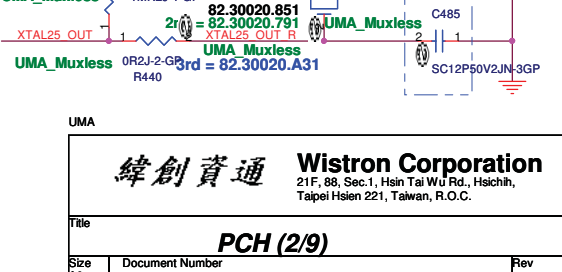
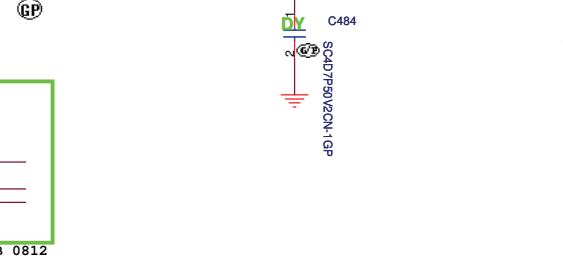
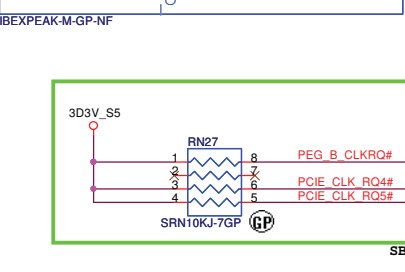
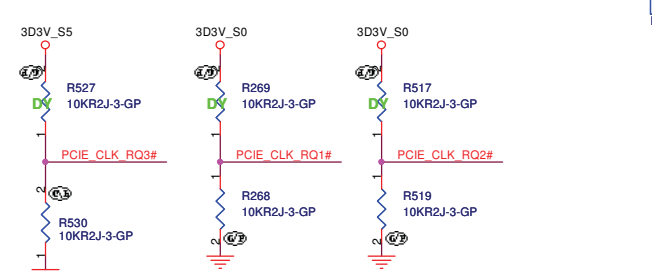
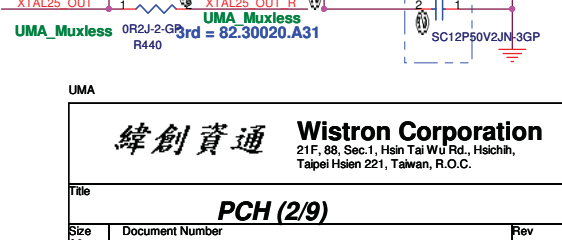
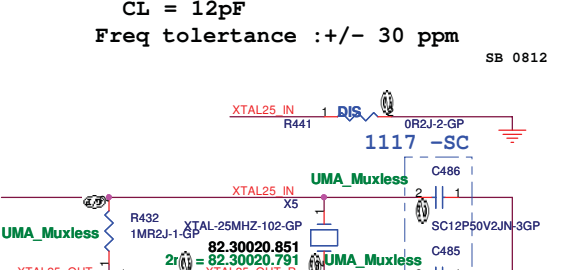
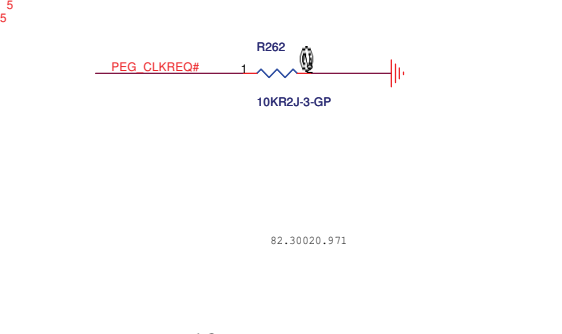
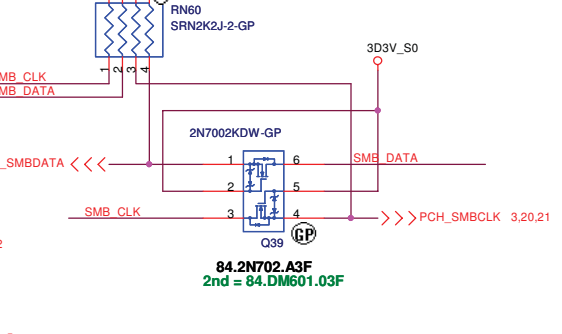
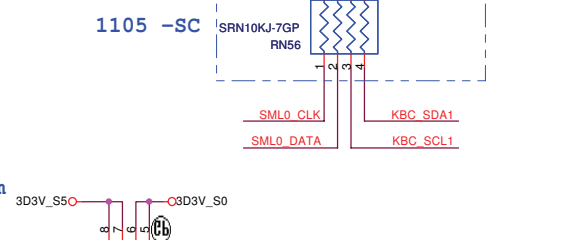
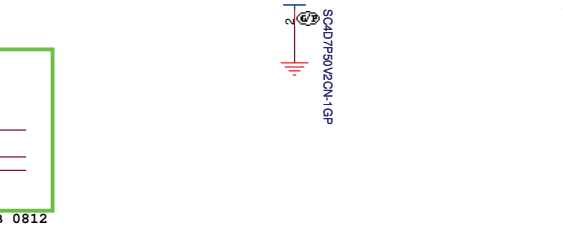
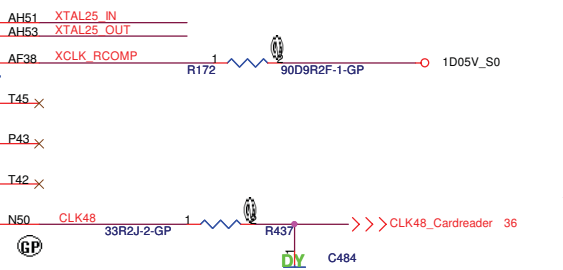
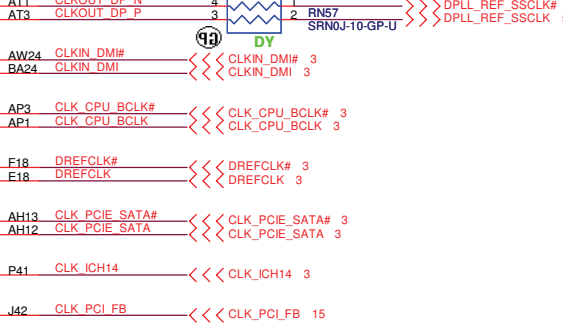
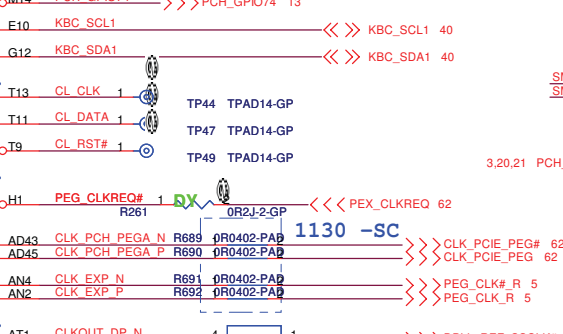
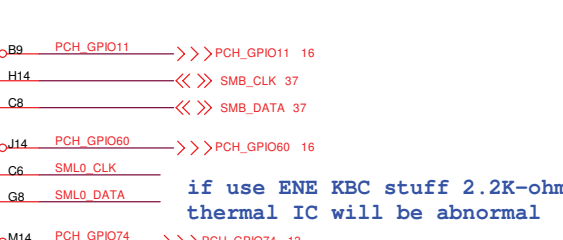
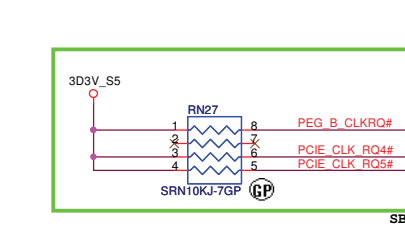
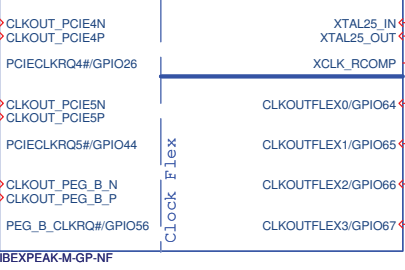
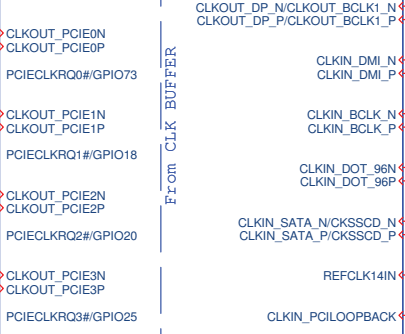
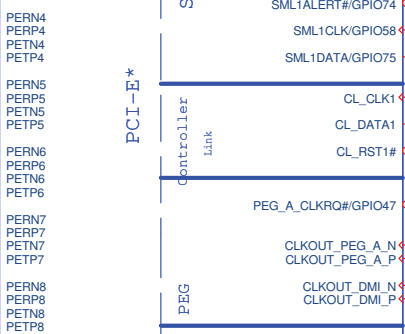
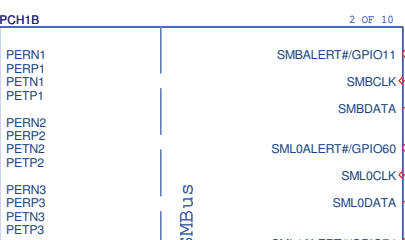
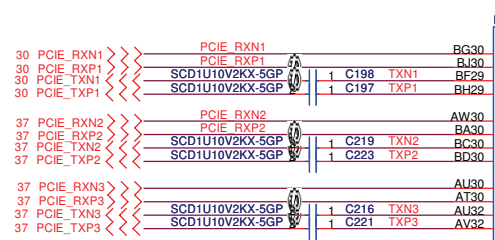
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LAN

MINICARD1

MINICARD2







Title			
<b>PCH (4/9)</b>			
Size A3	Document Number <b>HM42-CP</b>		Rev <b>SC</b>
Date: Friday, January 22, 2010		Sheet 14 of 72	





1209 -SC

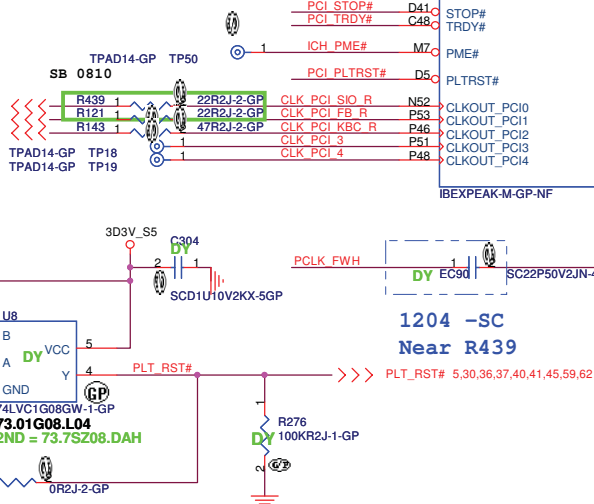


## PCH strapping

BOOT BIOS Strap		
GNT#0	GNT#1	BOOT BIOS Location
0	0	LPC
1	0	Reserved
floating	0	PCI
floating	floating	SPI (Default)

PCI_GNT#1	
1	Default (internal pull up)
0	Configures DMI for ESI compatible operation (Not for Mobile platform)

```
41 PCLK_FWH
12 CLK_PCI_FB
40 CLK_PCI_KBC
```




## PCH strapping

A16 swap override Strap/Top-Block  
Swap Override jumper

PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default
-----------	---

PCH strapping

NV_CLE	DMI termination voltage
floating	internal pull-up

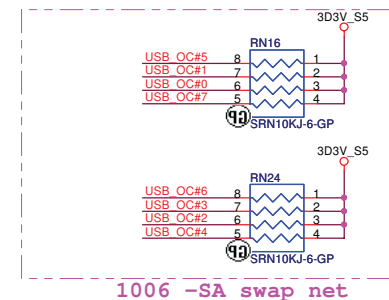
✗ These pins are left as NC,  because the function is disabled

NV_ALE	
1	Enable Anti-Theft Tech
floating	Disable (internal pull down)

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high

**USB**

Pair	Device
0	USB3
1	USB2
2	NC
3	MINICARD1 (WLAN)
4	WECAM
5	NC
6	NC
7	NC
8	3G SIM Card
9	USB1 (HS)
10	NC
11	Blue Tooth
12	MINIC2 (3G)
13	Cardreader



<Variant Name>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title
-------

**PCH (5/9)**

Size

Document Number

Date: Friday, January 22, 2010

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Rev  
SO



GPIO8 has a weak[20K] internal pull up.  
No need to have external pull down/up.  
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.  
No need to have external pull up/down.  
GPIO 15 pin is set to low at reset.  
Low : ME Crypto TLS with no confidentiality  
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.  
To enable on-die PLL Voltage regulator,  
should not place external pull down.

### HM42-CP\_NV\_Muxless SA

62 DGPU\_HOLD\_RST# >>> DGPU\_HOLD\_RST#  
55,61,62 DGPU\_PWROK >>> DGPU\_PWROK

TPAD14-GP TP36  
TPAD14-GP TP46  
TPAD14-GP TP45  
TPAD14-GP TP56

12 PCH\_GPIO11 <<< PCH\_GPIO11  
EC\_SW# <<< EC\_SW#  
12 PCH\_GPIO60 <<< PCH\_GPIO60  
PCH\_GPIO28 <<< PCH\_GPIO28

SRN10KJ-7GP  
PCH\_GPIO45 <<< PCH\_GPIO45  
R508 8K2R2J-3-GP

SB 0819  
PCH\_GPIO15 <<< PCH\_GPIO15  
R266 1KR2J-1-GP

PSW\_CLR# <<< PSW\_CLR#  
GAP-OPEN

11,44 SATA\_LED# <<< SATA\_LED#  
PCH\_GPIO39 <<< PCH\_GPIO39  
INT\_SERIRQ <<< INT\_SERIRQ  
PSW\_CLR# <<< PSW\_CLR#

SRN10KJ-7GP  
3D3V\_S0

STP\_PCI# <<< STP\_PCI#  
PCH\_GPIO22 <<< PCH\_GPIO22  
PCH\_GPIO0 <<< PCH\_GPIO0  
dGPU\_EDID <<< dGPU\_EDID

3D3V\_S0 <<< 3D3V\_S0  
SRN10KJ-L3-GP

PCH\_GPIO35 <<< PCH\_GPIO35  
10KR2J-3-GP R265

SB 0722  
AFTE14P-GP TP806  
AFTE14P-GP TP88

1 PCH TP95  
1 PCH TP96

AFTE14P-GP TP87  
AFTE14P-GP TP82

1 PCH TP97  
1 PCH TP98

AFTE14P-GP TP87  
AFTE14P-GP TP82

1 PCH TP97  
1 PCH TP98

AFTE14P-GP TP87  
AFTE14P-GP TP82

1 PCH TP97  
1 PCH TP98

AFTE14P-GP TP87  
AFTE14P-GP TP82

1 PCH TP97  
1 PCH TP98

AFTE14P-GP TP87  
AFTE14P-GP TP82

1 PCH TP97  
1 PCH TP98

AFTE14P-GP TP87  
AFTE14P-GP TP82

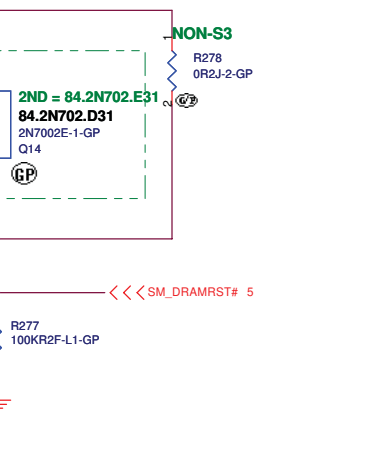
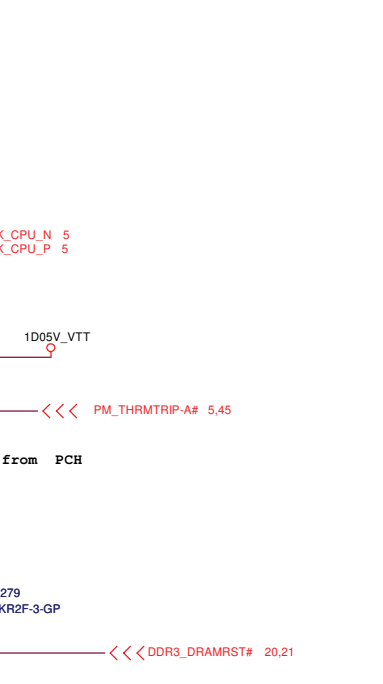
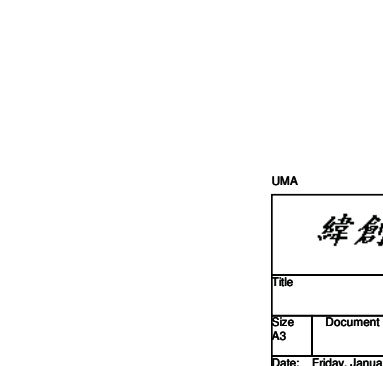
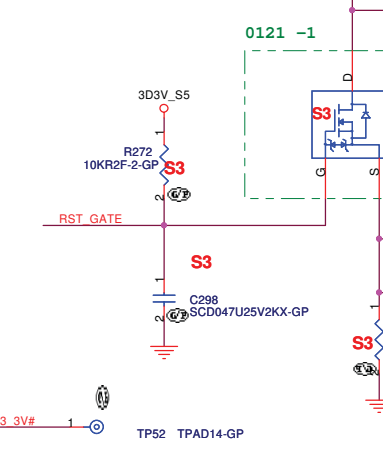
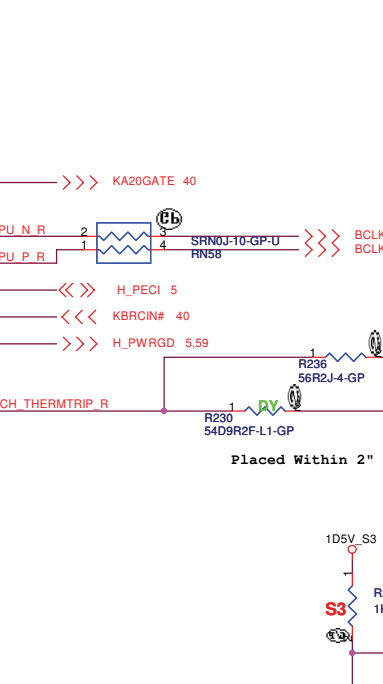
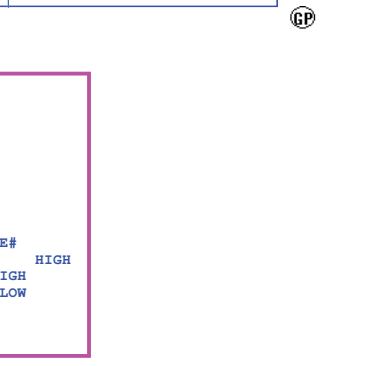
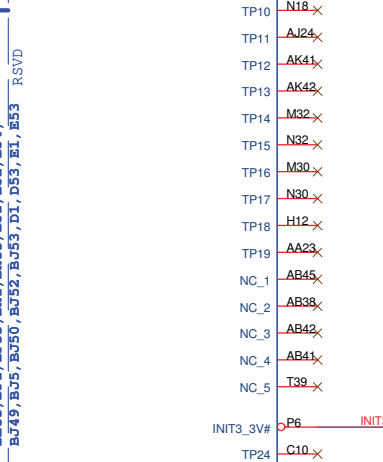
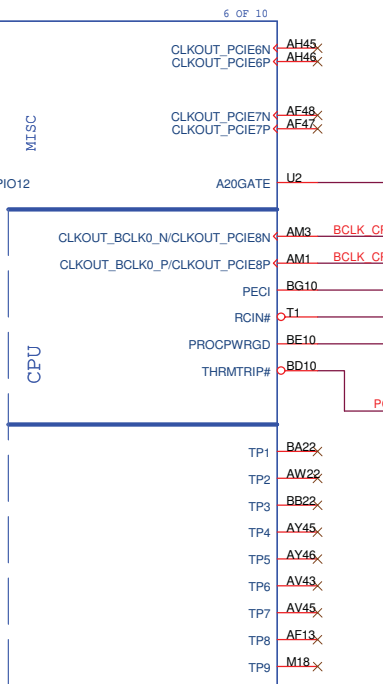
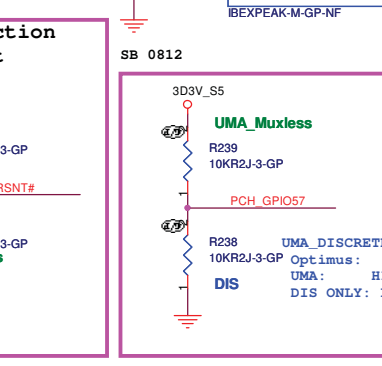
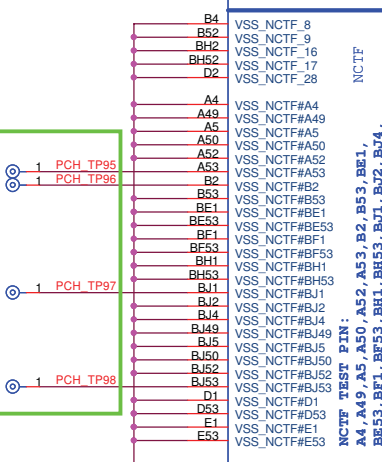
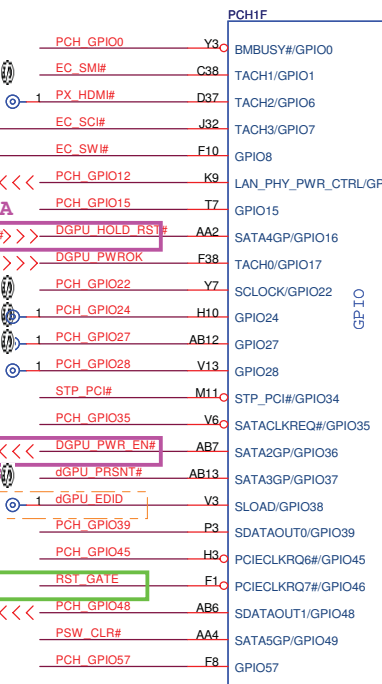
1 PCH TP97  
1 PCH TP98

AFTE14P-GP TP87  
AFTE14P-GP TP82

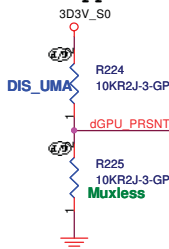
1 PCH TP97  
1 PCH TP98

AFTE14P-GP TP87  
AFTE14P-GP TP82

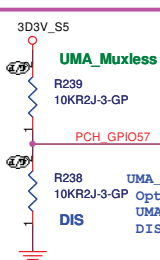
1 PCH TP97  
1 PCH TP98



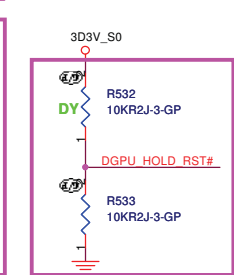
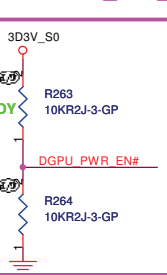
H: No SG function  
L: SG Support



SB 0812

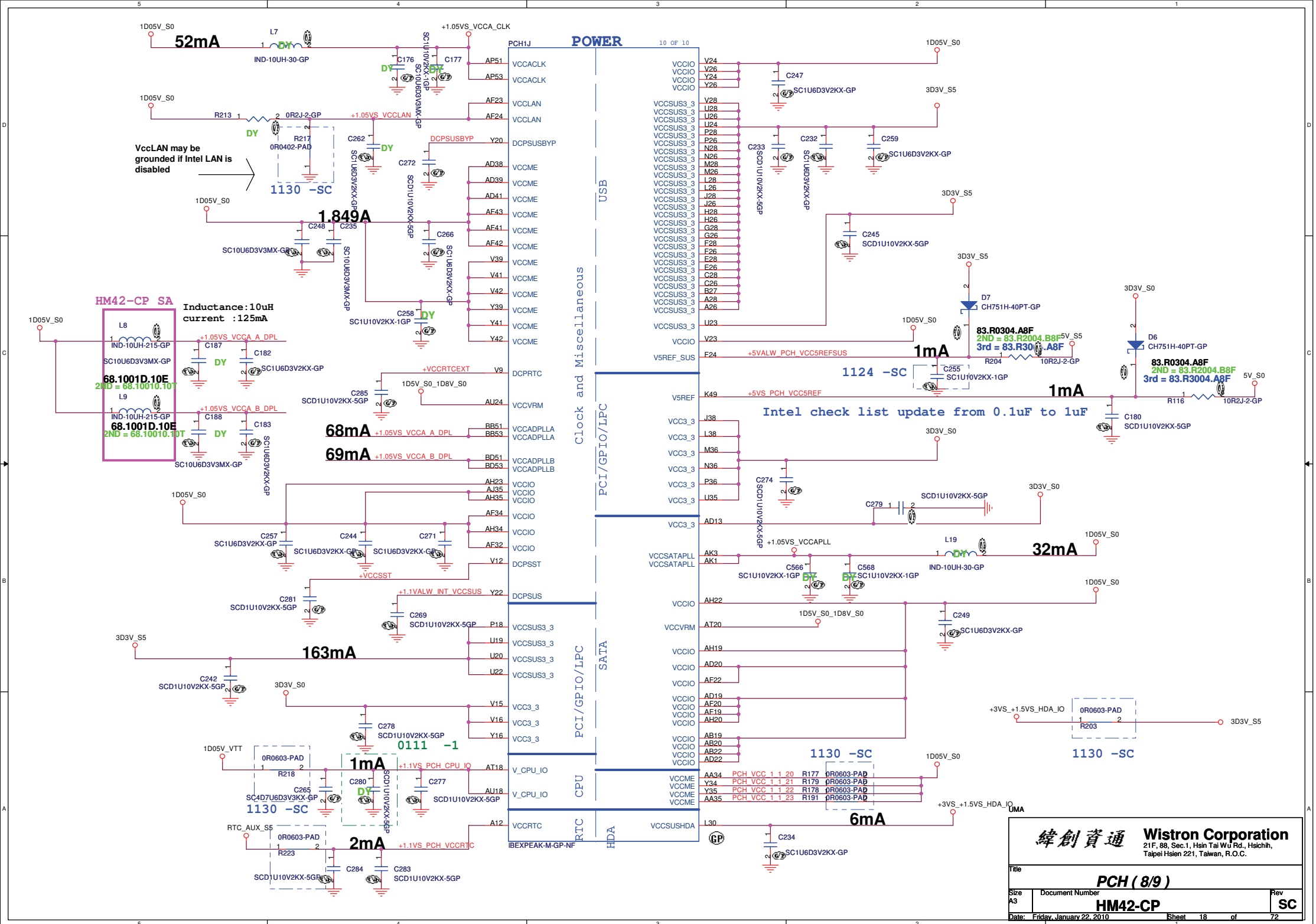


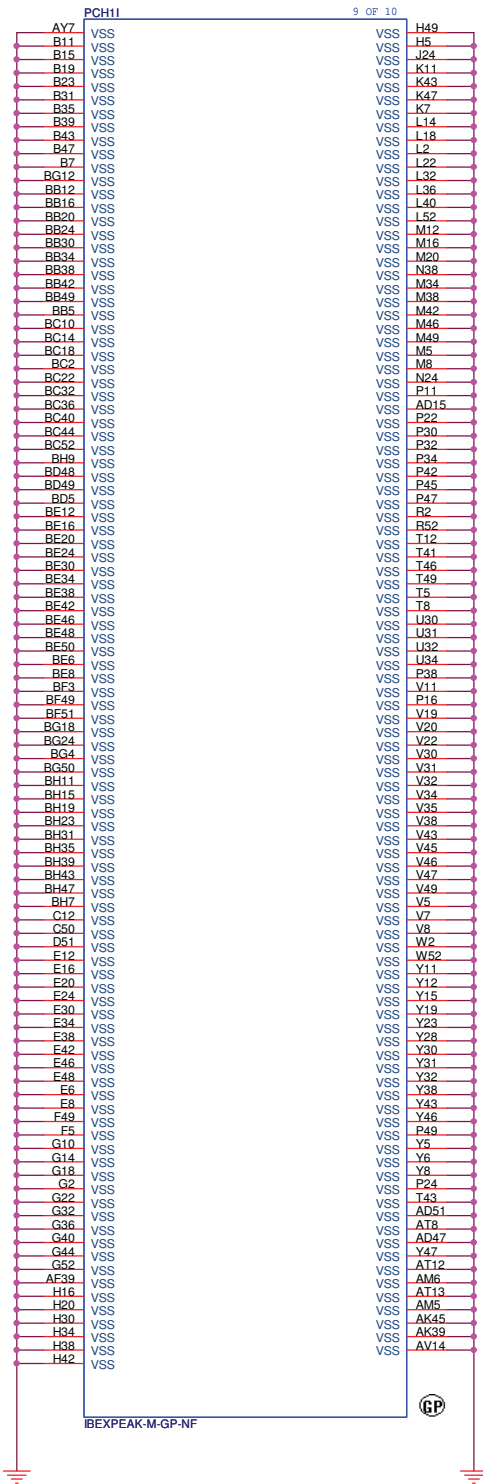
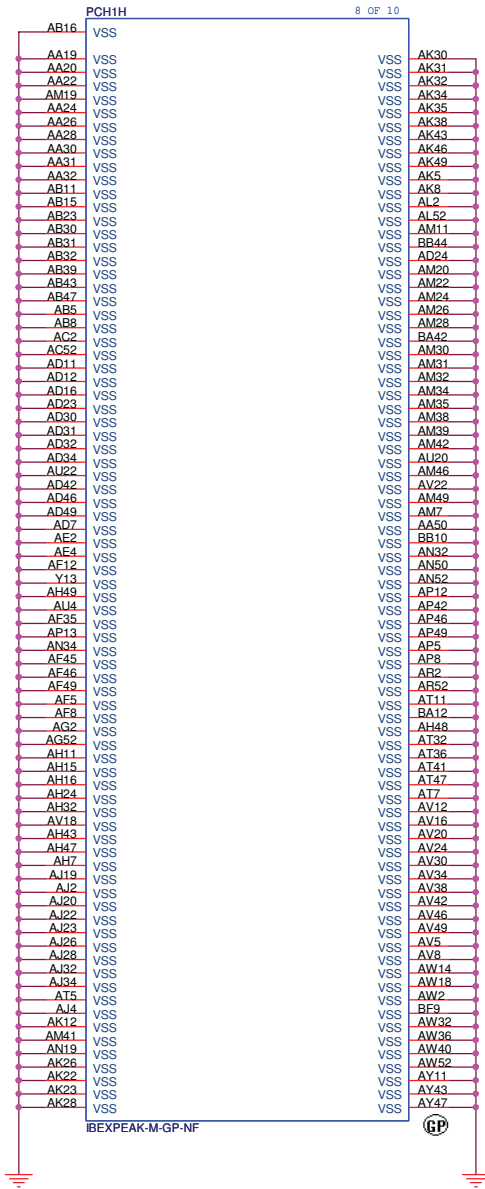
### HM42-CP\_NV\_Muxless SA

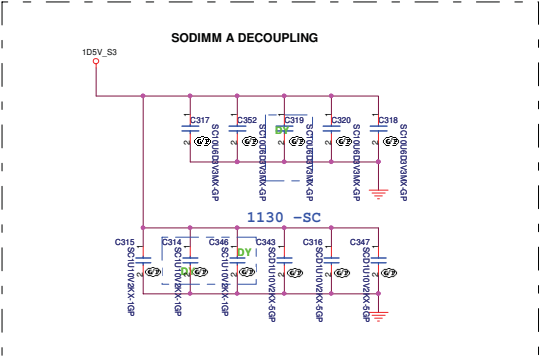
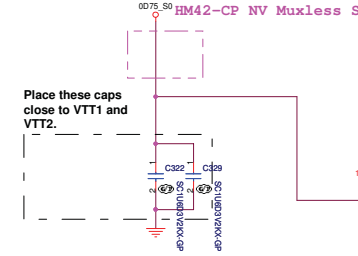


UMA

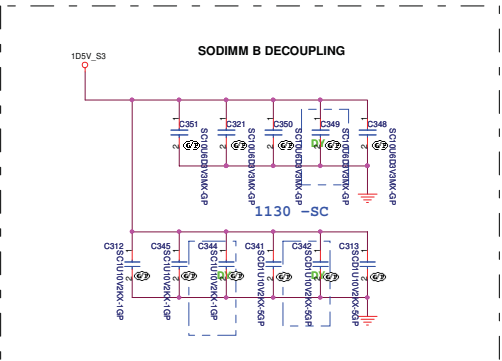




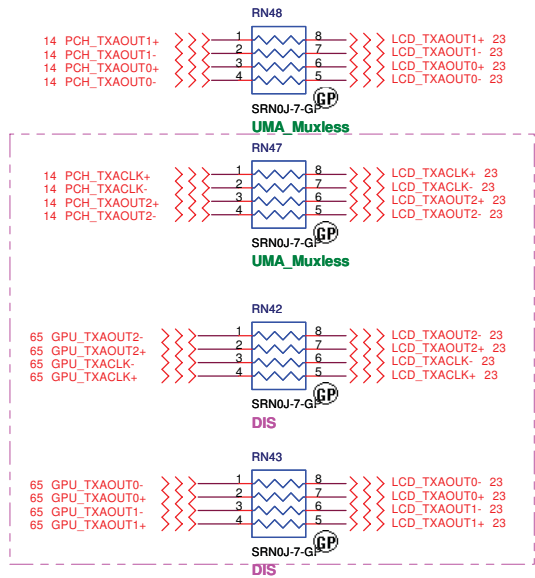




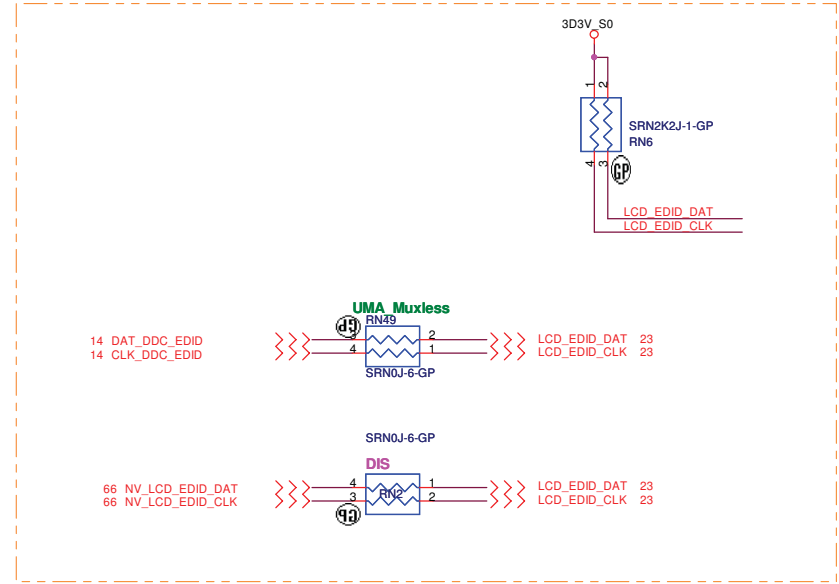
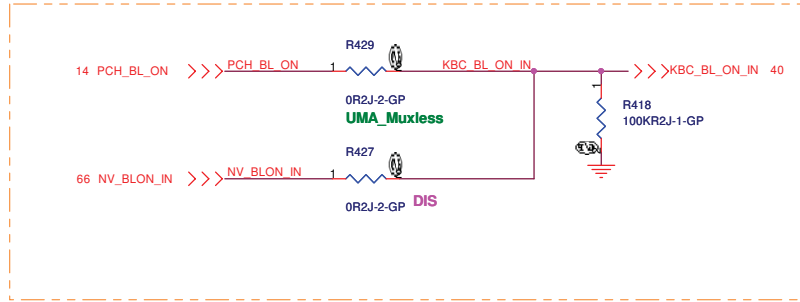
**Layout Note:**  
Place these Caps near  
SO-DIMMA.



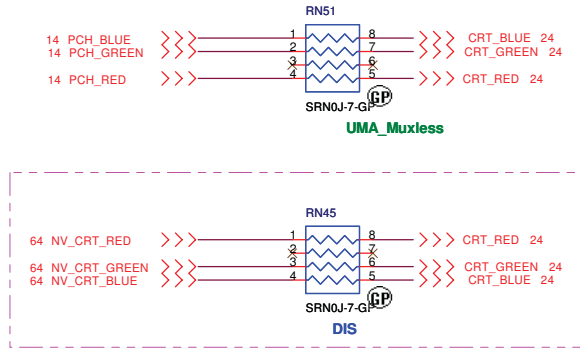
**SO-DIMMB is placed farther from the Processor than SO-DIMMA**



1016 -SB



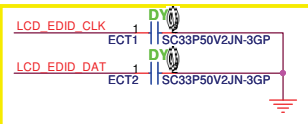
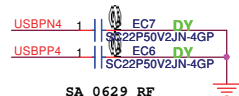
1016 -SB



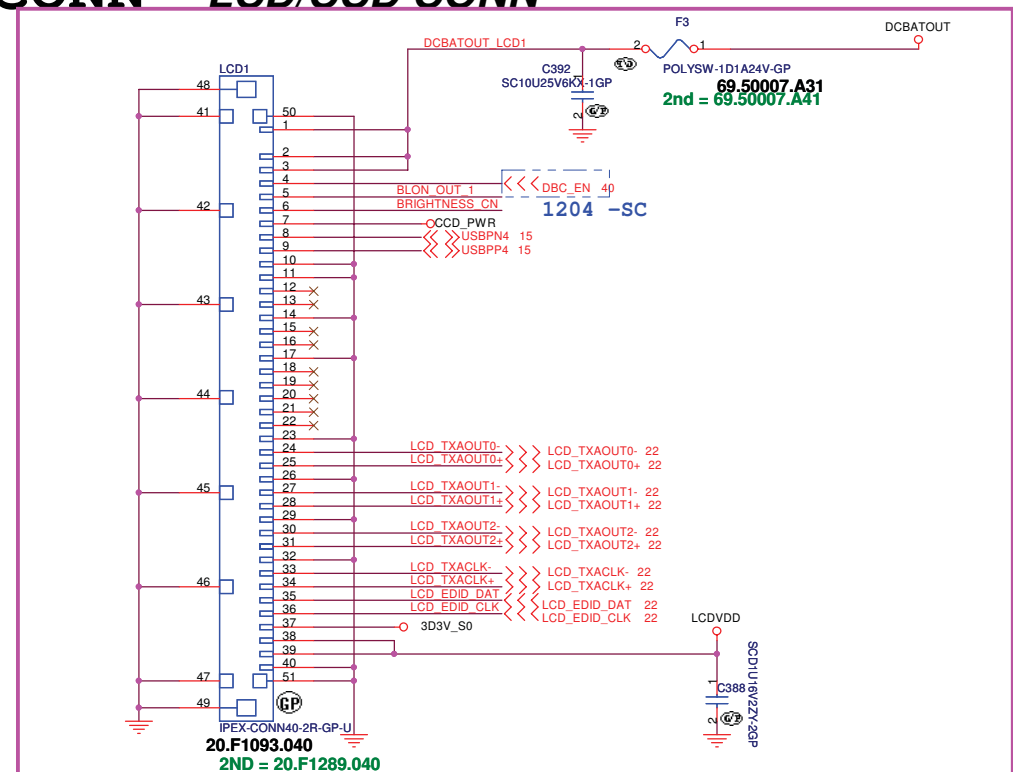
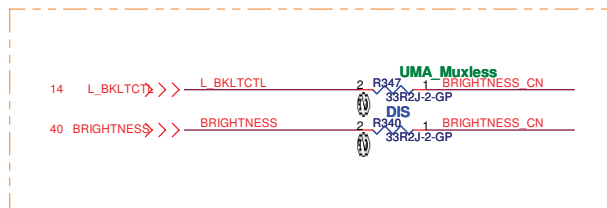


# LCD/INVERTER/CCD CONN

## LCD/CCD CONN

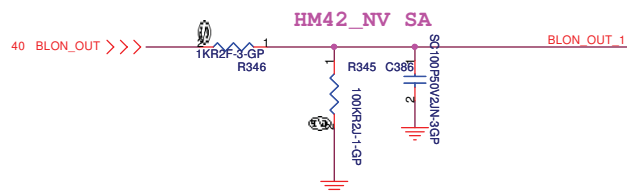


1016 -SB

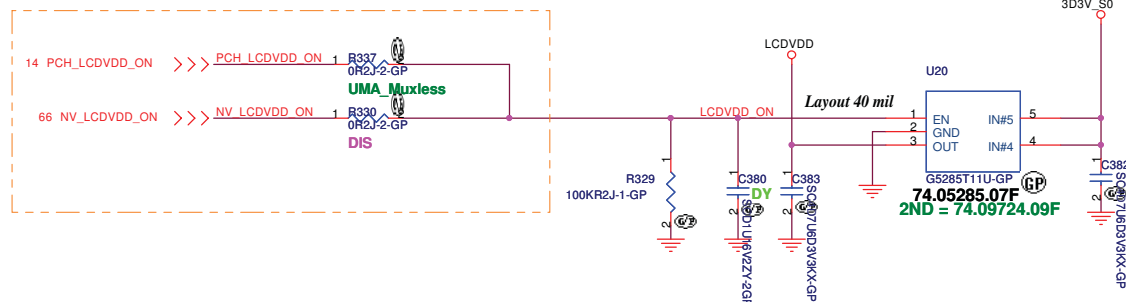


1005 -SA

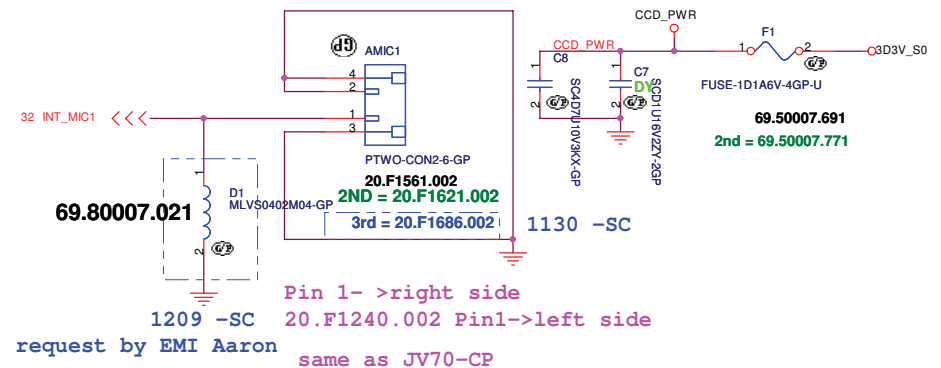
define same as SJM50-PU, can use SJM50 Cable



1016 -SB



## Internal Mic

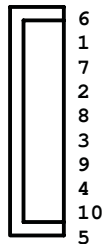


Discrete N11M

<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>LCD CONN</b>		
Size	Document Number <b>HM42-CP</b>	Rev <b>SC</b>
Date: Friday, January 22, 2010	Sheet 23 of 72	

[illegible]

## ***CRT I/F & CONNECTOR***



The schematic diagram illustrates the internal circuitry of the HM42 SA video output stage. It features two input multiplexers, UMA\_Muxless, which route NV and PCH signals to two comparators, U38B and U38C. The comparators are configured with various resistors (RN46, RN50, R521, R504, R494) and capacitors (C567, C568). The output of the comparators is connected to a driver stage, U38D, which drives the 1118-SC output. The circuit is powered by a 5V supply (S0) and includes a ground connection (GND).

**DDC\_CLK & DATA level shift**

**HM42 SA**

14 PCH\_DDCDATA  
14 PCH\_DDCCLK

64 NV\_CRT\_DDCDATA  
64 NV\_CRT\_DDCCLK

**DDC Circuit Components:**

- Resistors:** RN52 (SRN0J-6-GP), RN7 (SRN2K2J-1-GP), RN63 (SRN10KJ-5-GP)
- Capacitors:** C4, C5
- Diodes:** D9 (RB551V30-GP)
- Level Shifter:** Q42 (2N7002KDW-GP)
- Buffer:** Q43 (2N7002A3F)
- Fuse:** F2 (FUSE-1D1A6V-4GP-U)

**Power Supplies:** 3D3V\_S0, 5V\_CRT\_S0

**Output Signals:** DDCDATA, DDCCLK, DAT\_DDC1\_5, CLK\_DDC1\_5

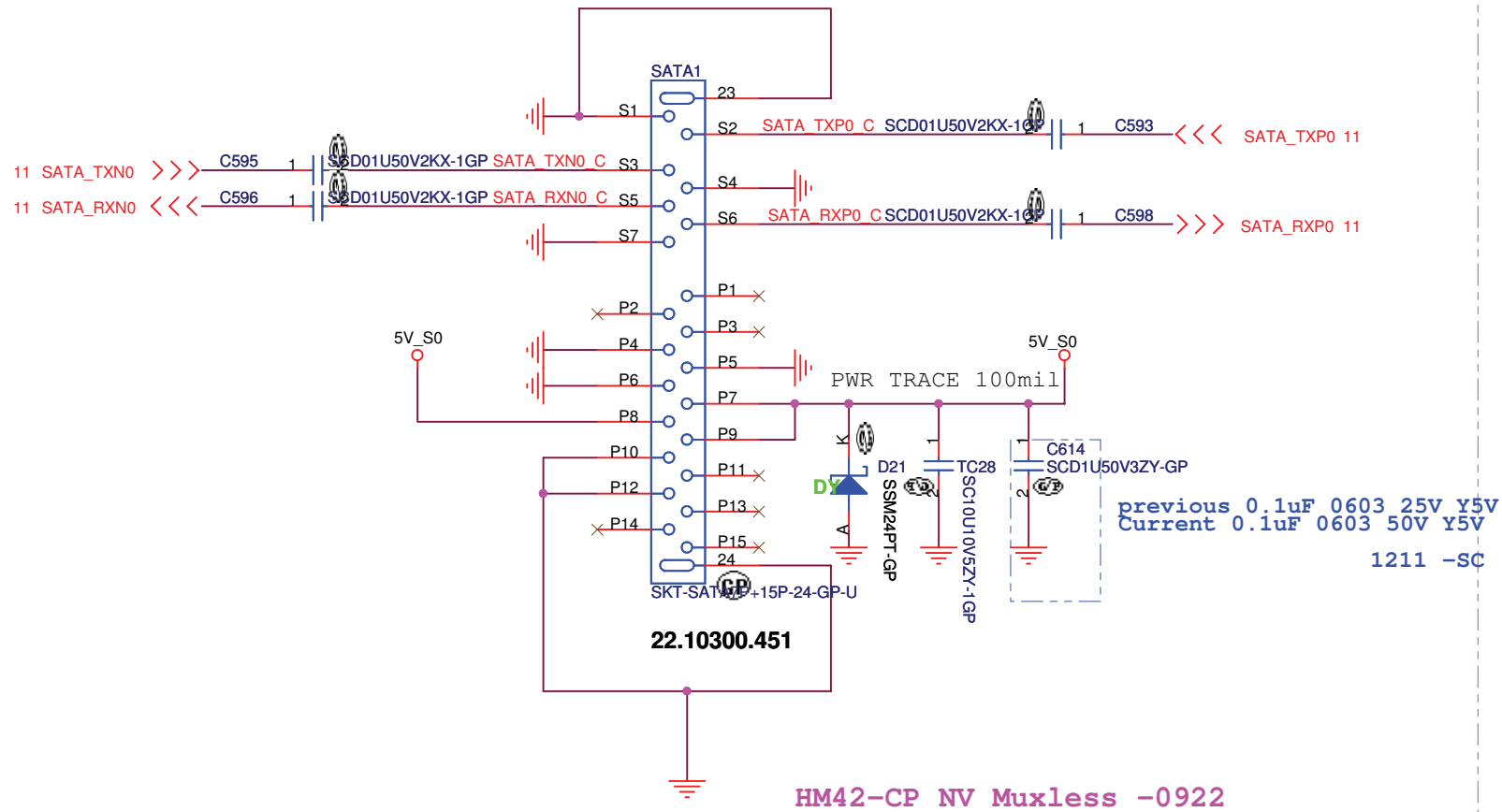
**Component Values and Part Numbers:**

- 69.50007.691  
2nd = 69.50007.771
- 1019 -SB
- 500mA
- 2ND = 83.5R003.08F
- 83.R5003.H8H
- 3rd = 83.R5003.C8F
- 84.2N702.A3F
- 2nd = 84.DM601.03F

Title			
<b>CRT CONN</b>			
Size	Document Number		Rev
	<b>HM42-CP</b>		<b>SC</b>
Date:	Friday, January 22, 2010	Sheet 24 of	72



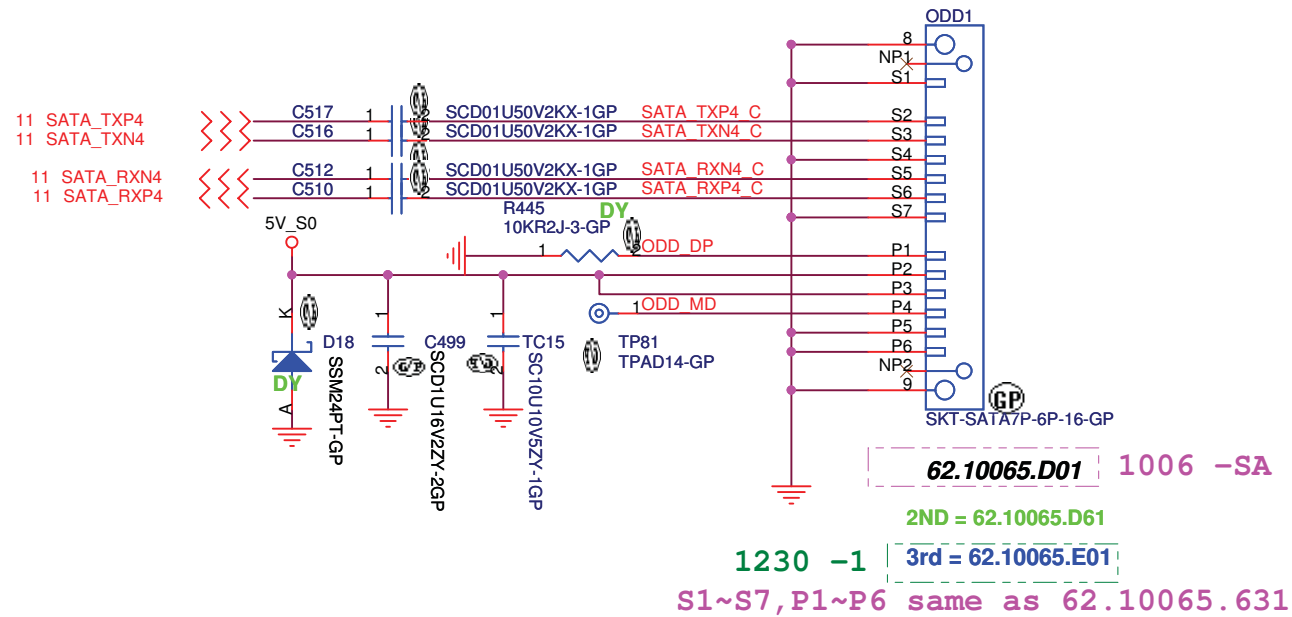
# SATA Connector



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
HDD CONN	
Size	Document Number
	HM42-CP
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Rev	SC

# ODD Connector



UMA

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**ODD**

Size

Document Number

**HM42-CP**

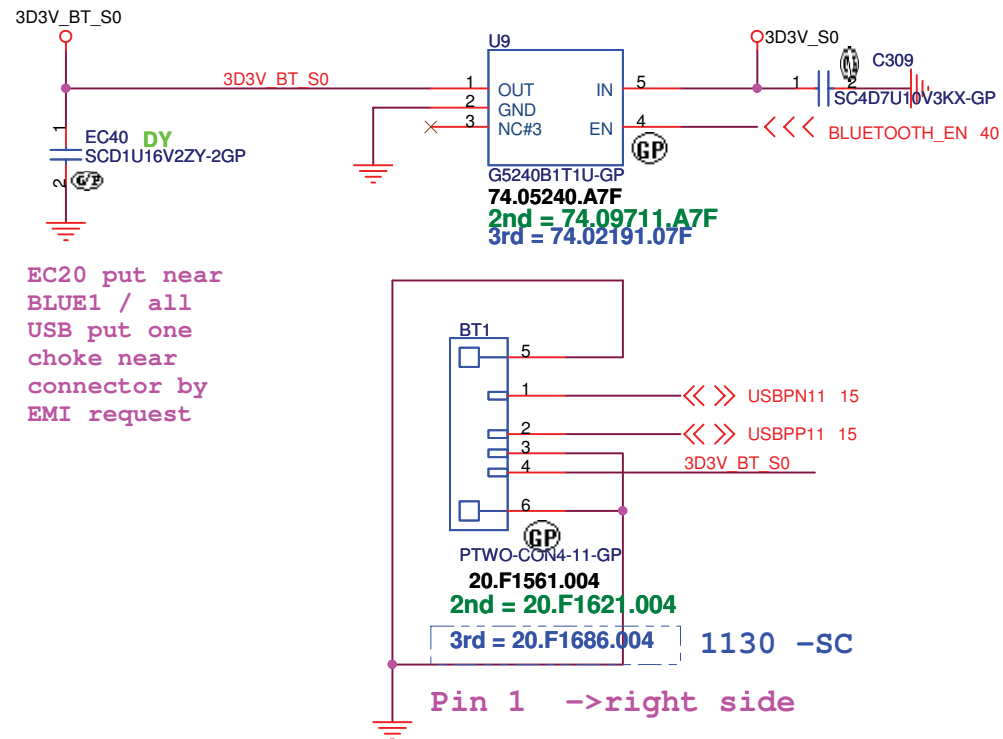
Rev

SC

Date: Friday, January 22, 2010

Sheet 27 of 72

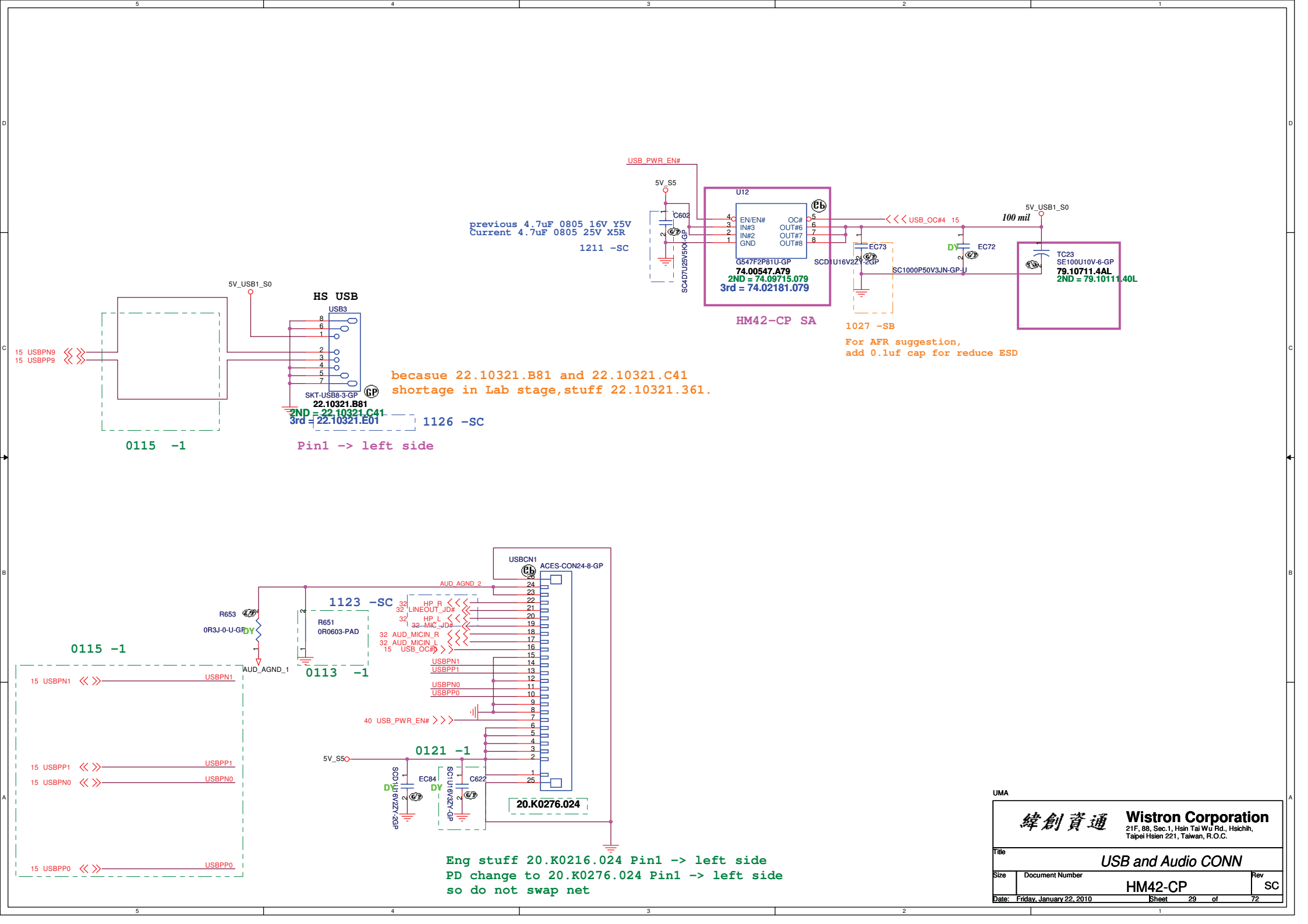
# BLUETOOTH MODULE



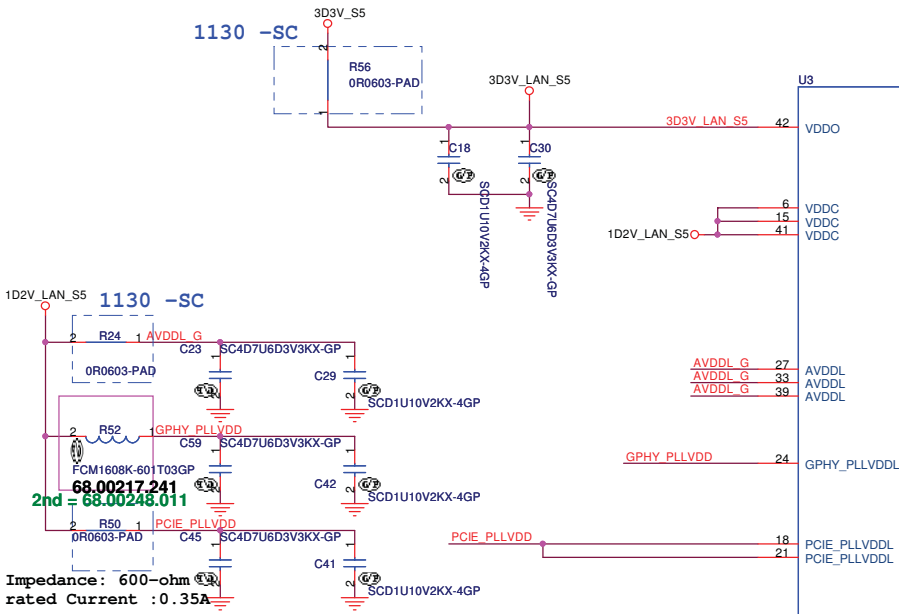
JV50

緯創資通 Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

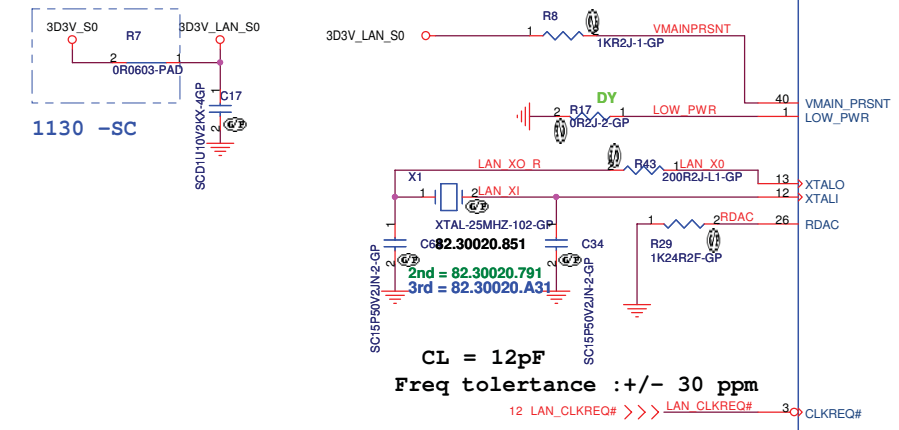
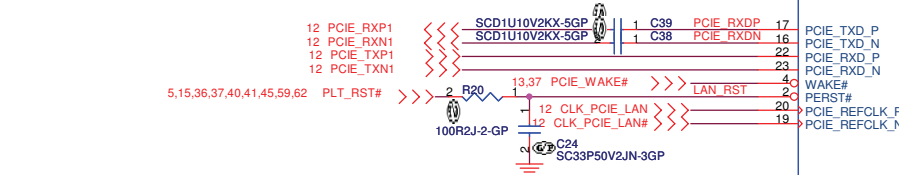
Title		
BLUETOOTH		
Size	Document Number	Rev
	HM42-CP	SC
Date:	Friday, January 22, 2010	Sheet 28 of 72



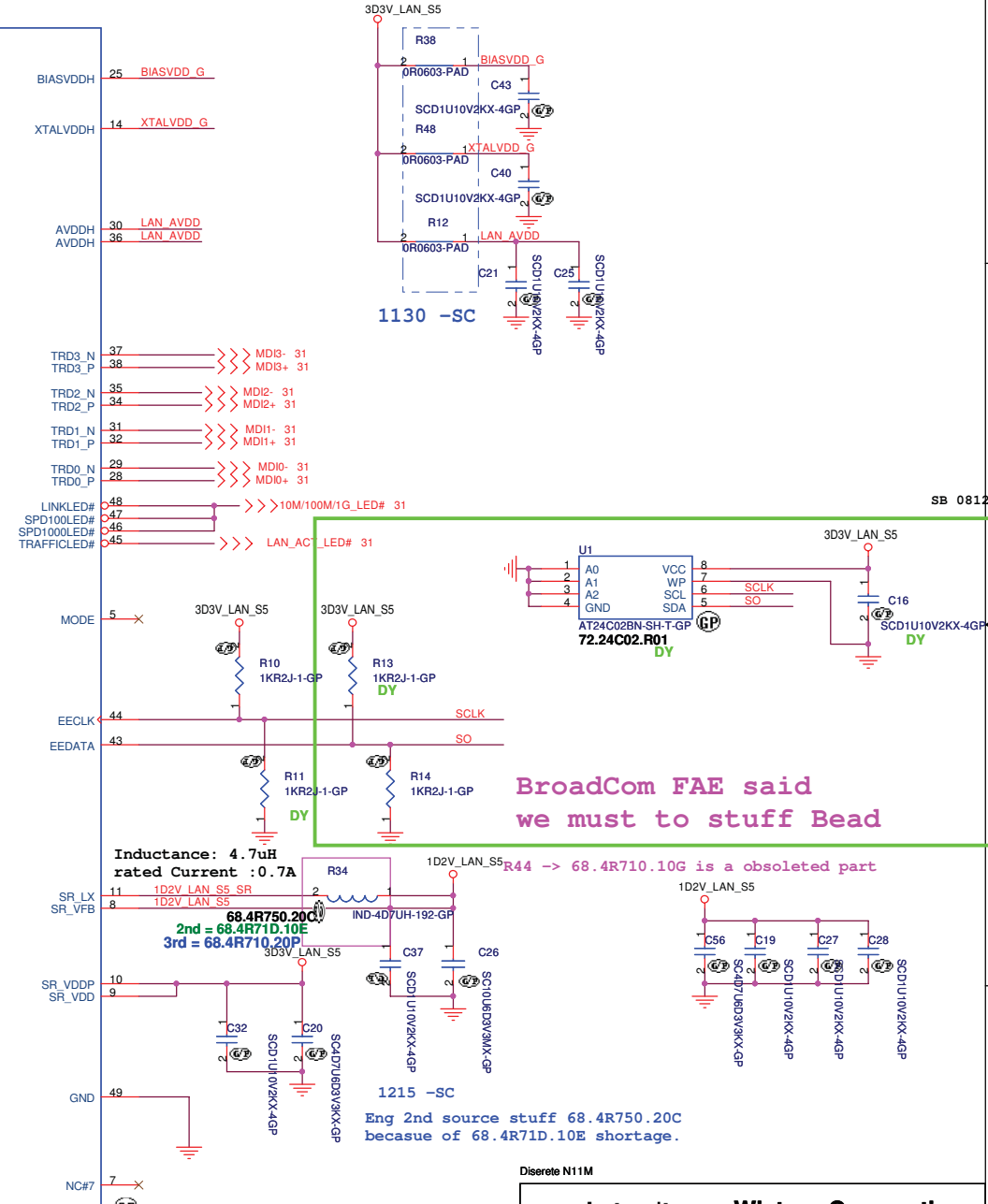




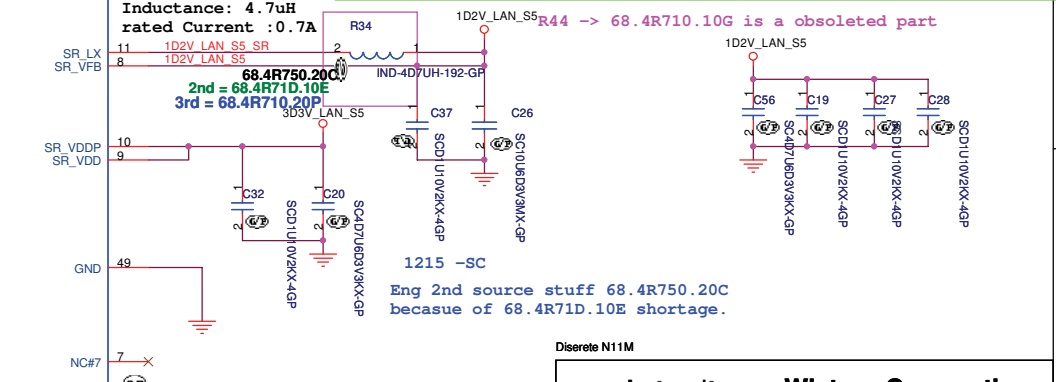
BroadCom FAE said  
we must to stuff Bead



71.57780.M04



BroadCom FAE said  
we must to stuff Bead



Discrete N11M

緯創資通 Wistron Corporation

21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

BCM57780

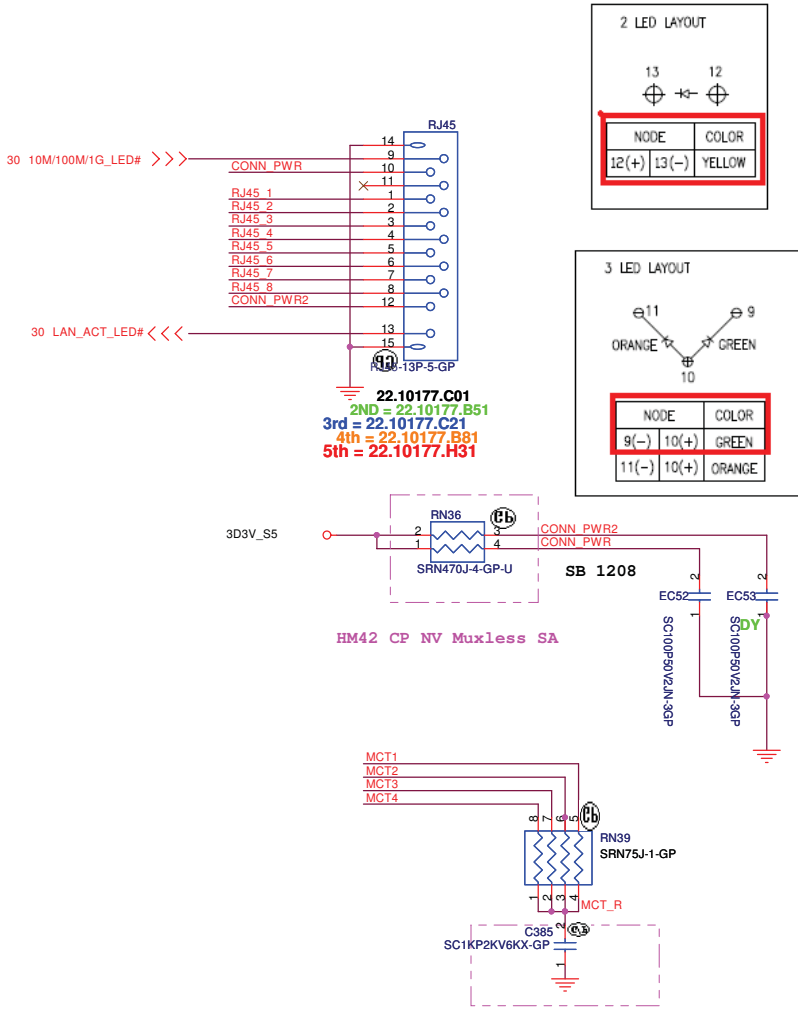
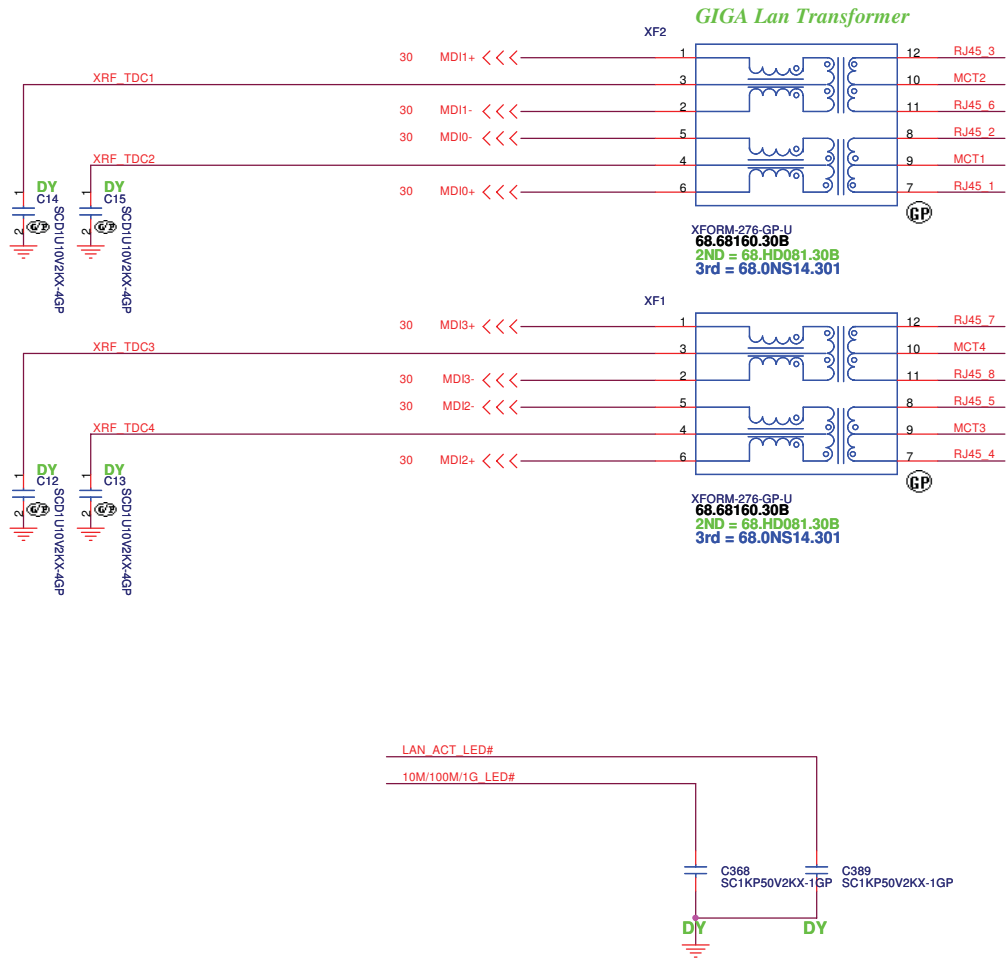
Size A3 Document Number HM42-CP Rev SC

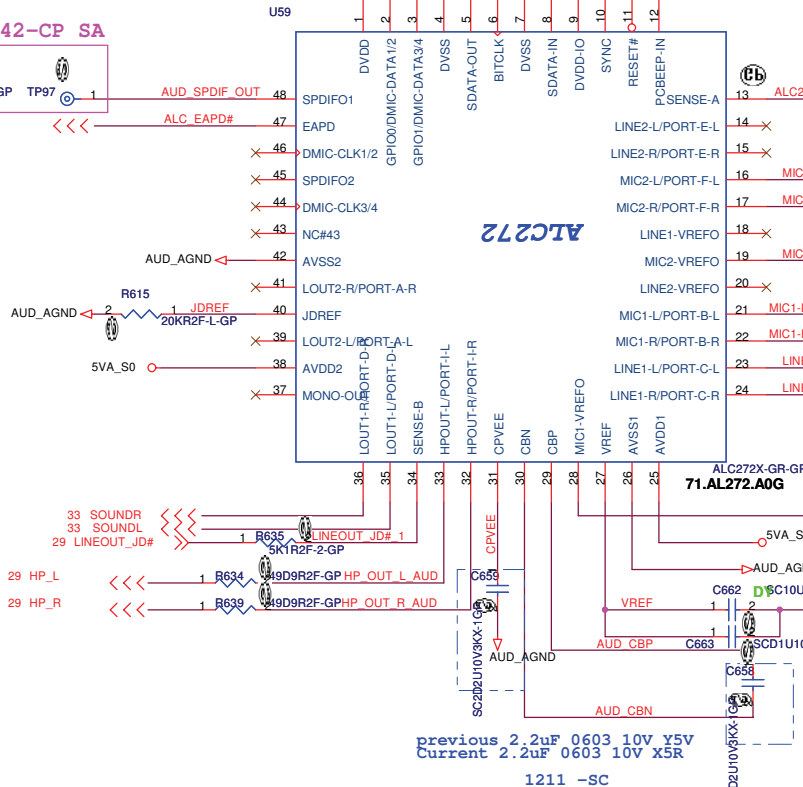
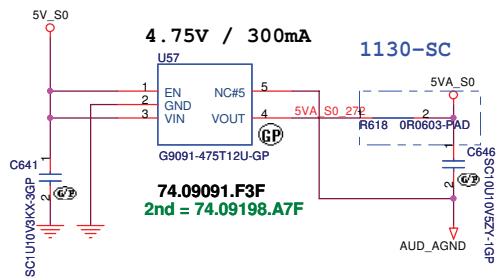
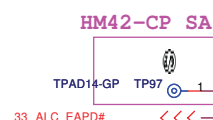
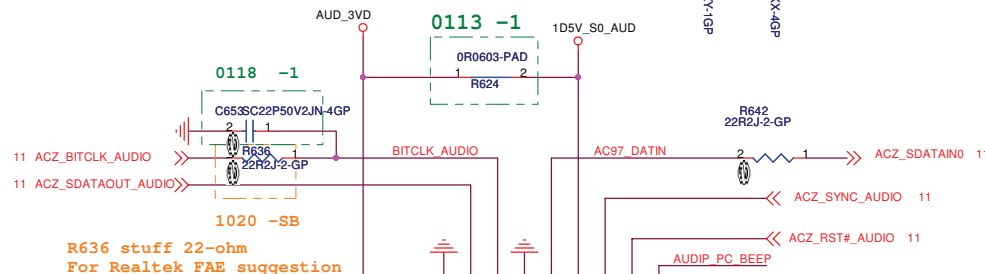
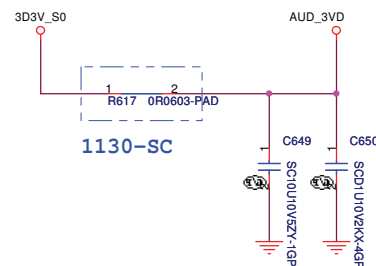
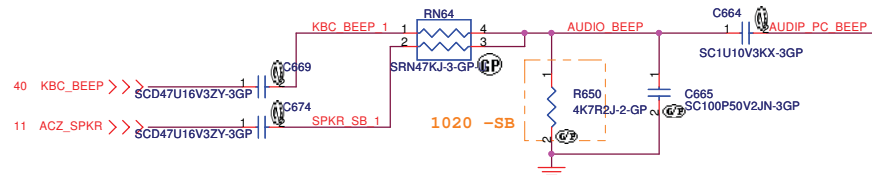
Date: Friday, January 22, 2010 Sheet 30 of 72

- 1.route on bottom as differential pairs.  
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.  
3.No vias, No 90 degree bends.  
4.pairs must be equal lengths.  
5.6mil trace width, 12mil separation.  
6.36mil between pairs and any other trace.  
7.Must not cross ground moat,except RJ-45 moat.

# LAN Connector

# LAN Connector

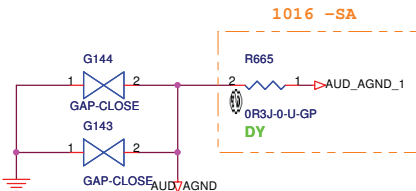


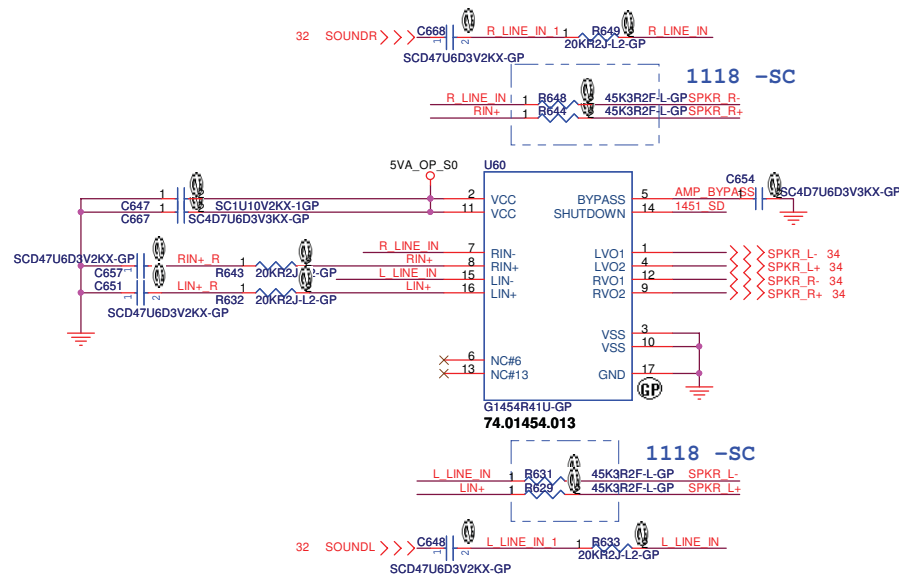
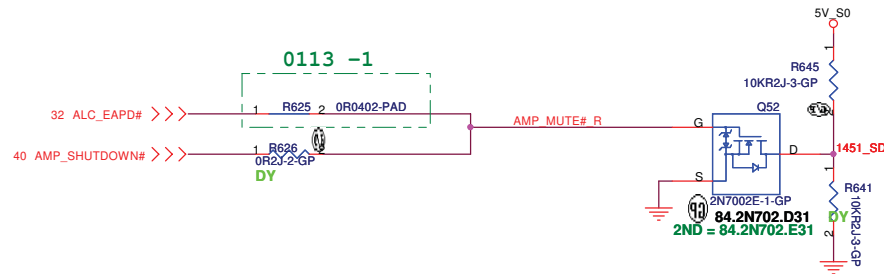
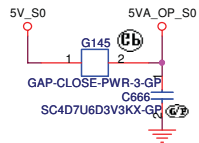


HM4-CP SA

0118 -1 EMI

83.00355.A1F  
2nd = 83.00355.D1F  
3rd = 83.00355.E1F

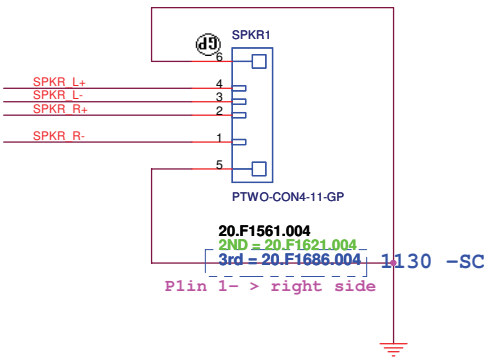
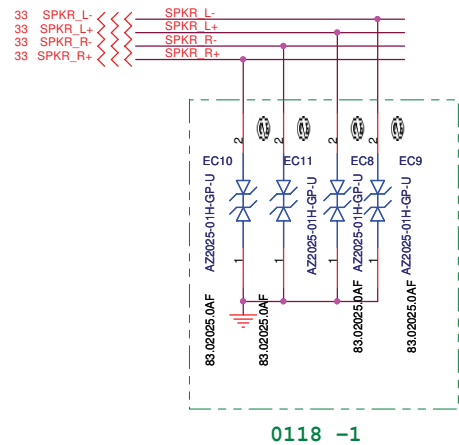




Gain=  $R_f/R_i=52K/20K=2.6V/V$   
 $f(HP)=1/(2 \pi * 20K * 0.47\mu f)=16.9Hz$   
 If  $V_{IN}=1.54V$  Gain=2.6V/V  $R_L=4\Omega$   $V_O(peak)=4V$   $V(rms)=2.828V$   
 Power=  $2.446^2/4=1.5W$

UMA

Internal Speaker



JV50

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Resrve MDC		
Size	Document Number	Rev
	HM42-CP	SC
Date: Friday, January 22, 2010		Sheet 35 of 72

Pin No.	SD/MMC	MS/MS PRO	xD
P20 MS-DATA1		3P	
P21 MS-BS		2P	
P22 4in1-GND	3P/6P	1P/10P	1P/9P
P23 SD-VCC	4P		
P24 SD-CLK	5P		
P25 SD-DAT0	7P		
P26 xD-D2			12P
P27 xD-D3			13P
P28 xD-D4			14P
P29 SD-DAT1	8P		
P30 xD-D5			15P
P31 xD-D6			16P
P32 xD-D7			17P
P33 xD-VCC			18P
P34 XD-CD-SW			19P
P35 SD-WP-SW	SD-WP-SW		
P36 SD-CD-SW	SD-CD-SW		
P37 4 IN 1-GND	SD-WP/CD-SW-GND		
P38			

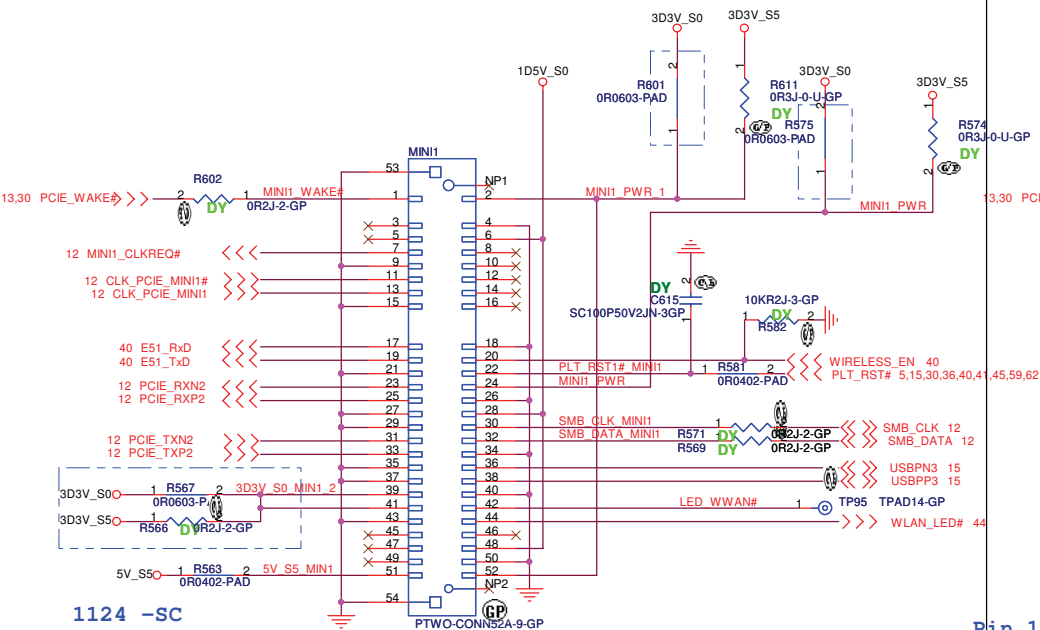
Pin	Name	Dir	description
1	XD_CD#	-	presence detect
2	R/B#	OUT	Ready / Busy (open-drain)
3	RE#	IN	Read Enable
4	CE#	IN	Card Enable
5	CLE	IN	Command Latch Enable
6	ALE#	IN	Address Latch Enable
7	WE#	IN	Write Enable
8	WP#	IN	Write Protect
9	GND	-	Ground
10	SD0	IN/OUT	data bit 0
11	SD1	IN/OUT	data bit 1
12	SD2	IN/OUT	data bit 2
13	SD3	IN/OUT	data bit 3
14	SD4	IN/OUT	data bit 4
15	SD5	IN/OUT	data bit 5
16	SD6	IN/OUT	data bit 6
17	SD7	IN/OUT	data bit 7
18	VCC	-	3.3V power

Pin	Pin Name	Description
1	VSS	Vss
2	BS	Bus state signal
3	DATA1	Data1 Parallel / NC Serial
4	SDIO/DATA0	Data0 Parallel / Data Serial
5	DATA2	Data2 Parallel / NC Serial
6	INS	Stick detect (connected to VSS)
7	DATA3	Data3 Parallel / NC Serial
8	SCLK	Clock signal
9	VCC	Vcc (2,7V - 3,6V)
10	VSS	Vss

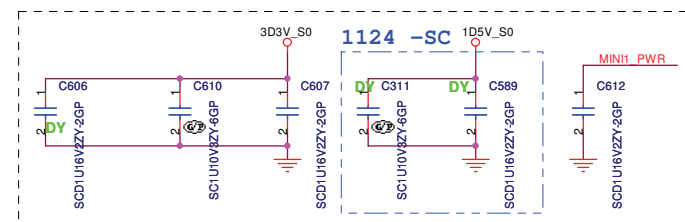


# Mini Card Connector(WLAN)

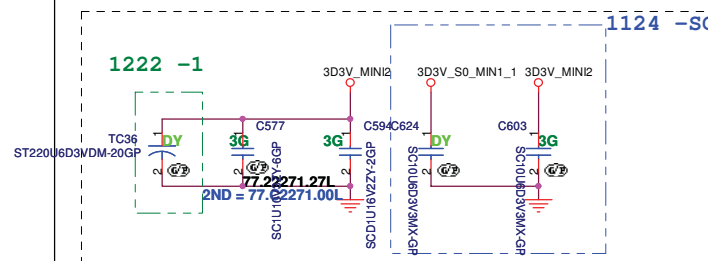
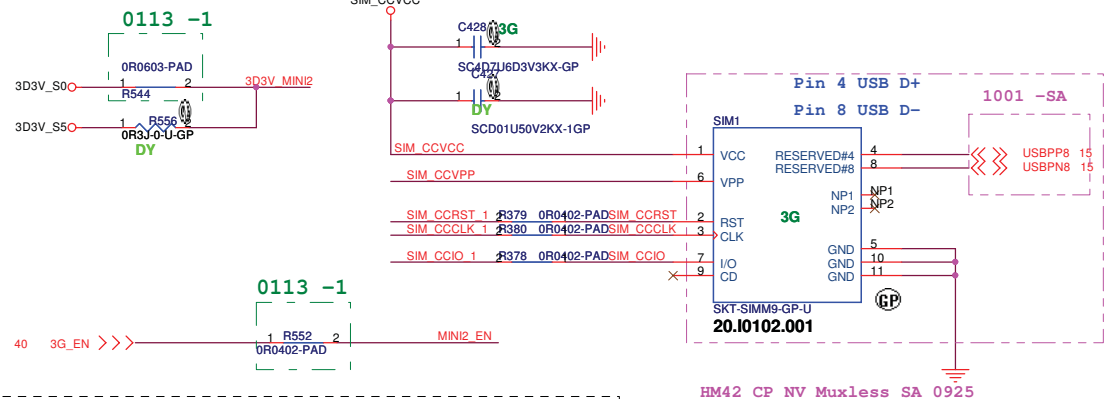
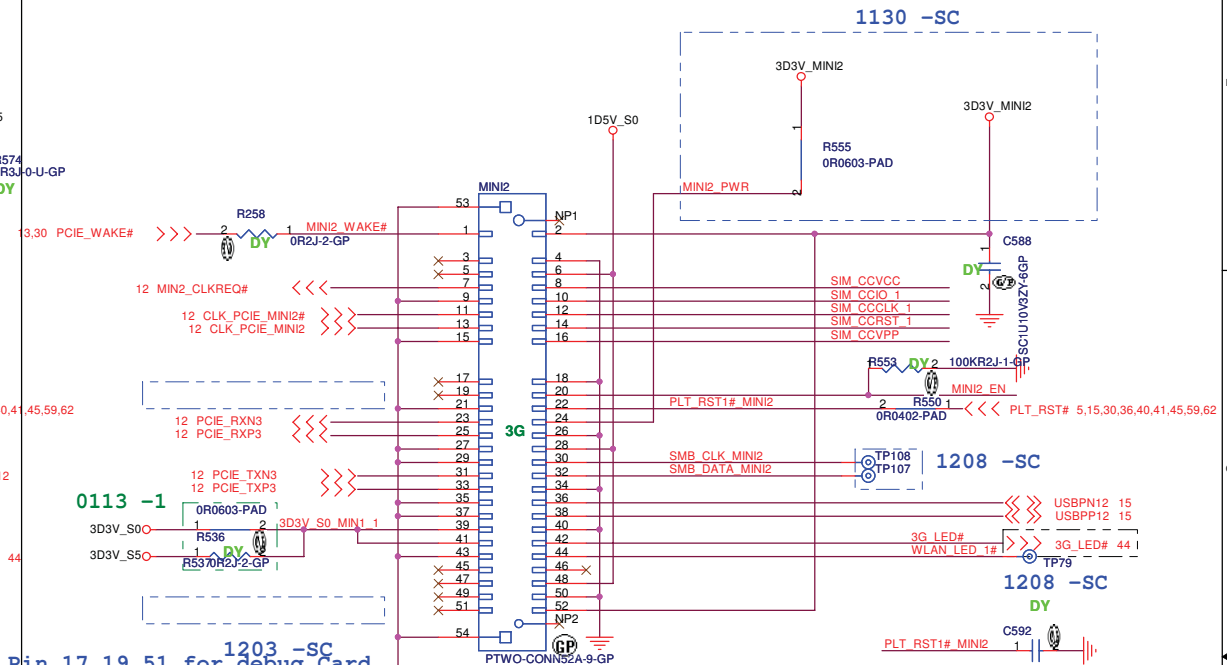
## Support debug-card



Place near MINI1



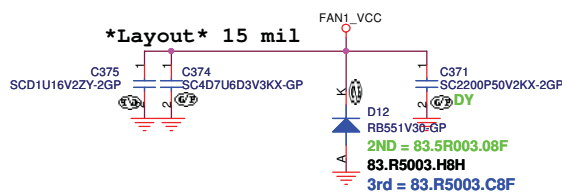
# Mini Card Connector(Robson2 and 3G)



Discrete N11M

緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

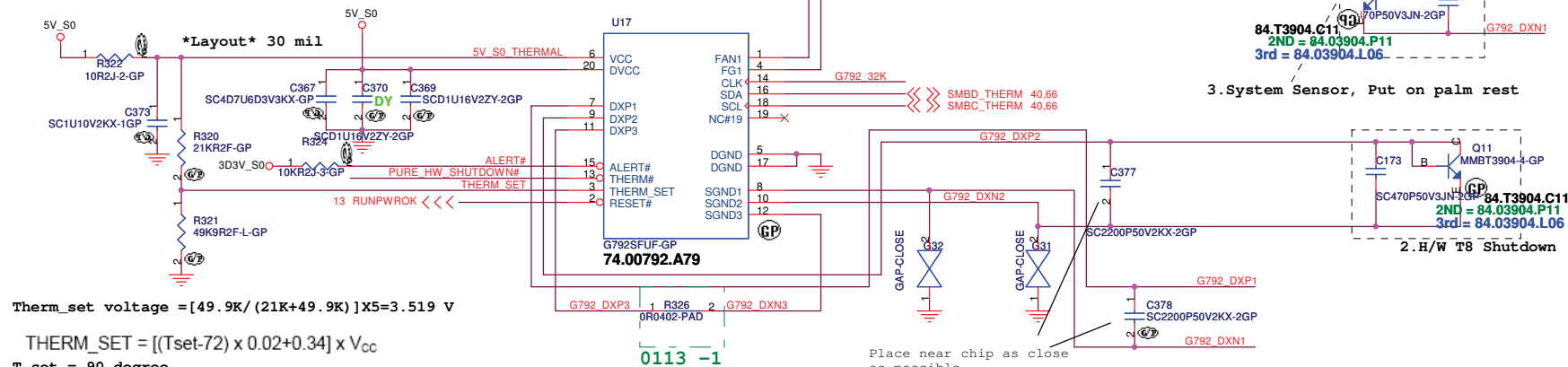
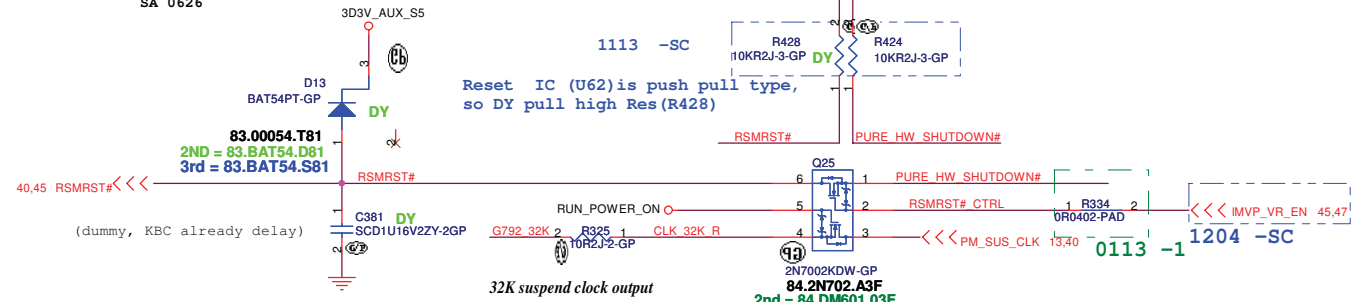
Title			MINI CARD
Size	Document Number	Rev	
A3	HM42-CP	SC	
Date:	Friday, January 22, 2010	Sheet	37 of 72



## Thermal Get define

- Sensor0 => CPU
- Sensor1=> system temp (thermal DPX1)
- Sensor2=> HW T8 shut down(thermal DPX2)
- Sensor3=> unused(thermal DPX3)
- Sensor4=> MCH
- Sensor5=> PCH
- Sensor6=> Adpater Current
- Sensor7=>dGPU
- Sensor8=>Battery Thermal
- Sensor9=>Battery Current

SA 0626



Therm\_set voltage = [49.9K/ (21K+49.9K)] x 5.519 V

THERM\_SET = [(Tset-72) x 0.02+0.34] x V<sub>CC</sub>

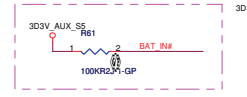
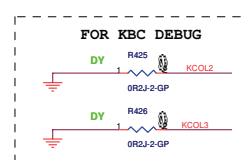
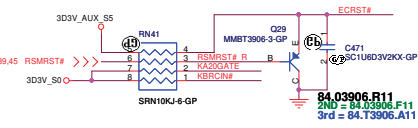
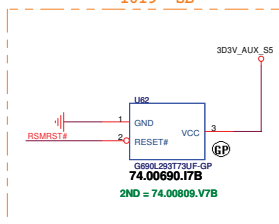
T set = 90 degree

therm\_set is 3.5V => [(90-72)x0.02+0.34]x5=3.5V

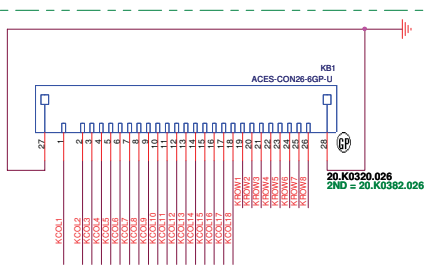
DXP1: System Sensor  
DXP2: H/W Setting (T8)  
DXP3: do not use

UMA

Prevent BIOS data loss solution  
1019 -SB

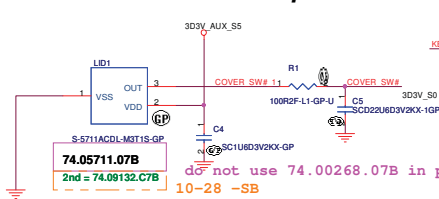


## Internal Keyboard Connector

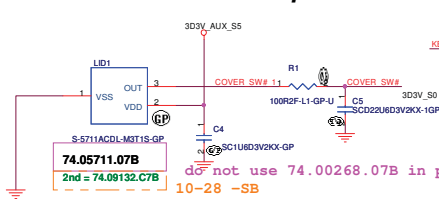


change connect to FPC (Same as Lab)  
20.K0251.026 Pin 1 -> left side  
20.K0320.026 Pin 1 -> right side (use in lab stage)  
so swap net

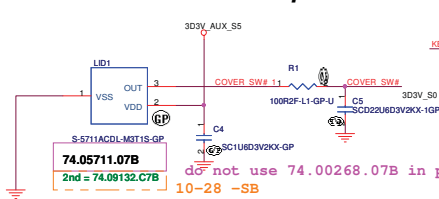
## Cover Up Switch



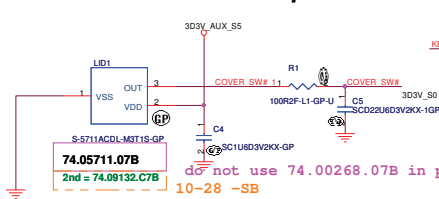
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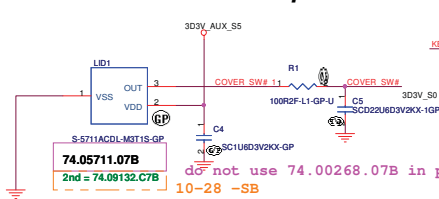
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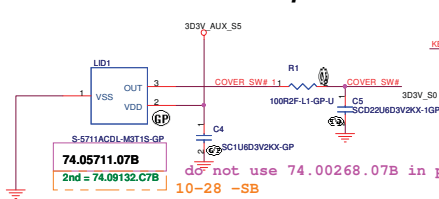
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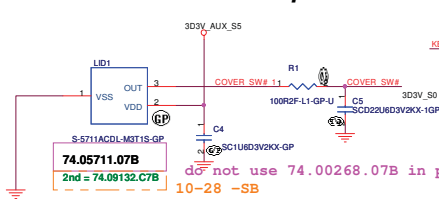
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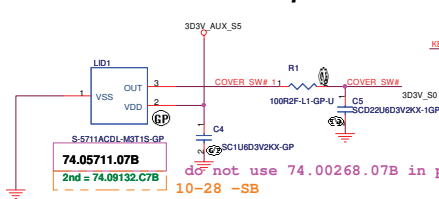
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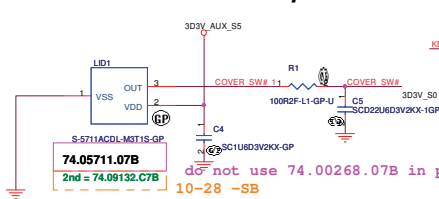
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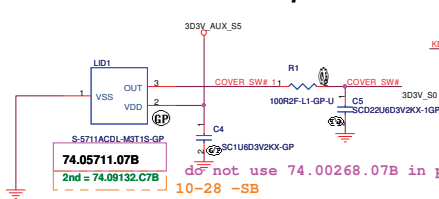
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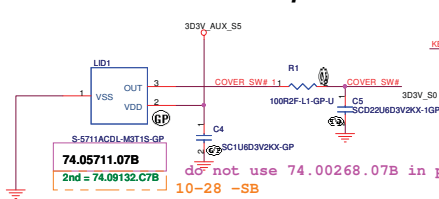
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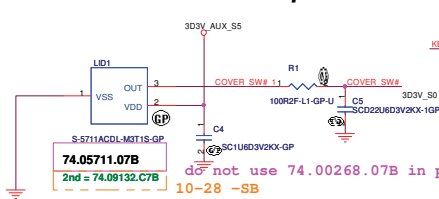
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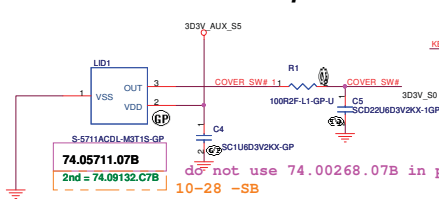
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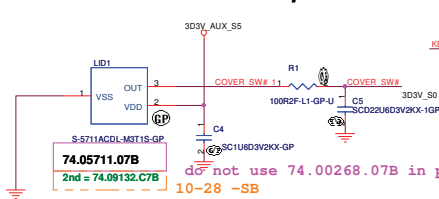
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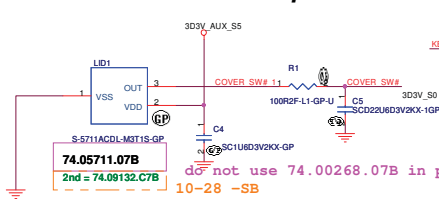
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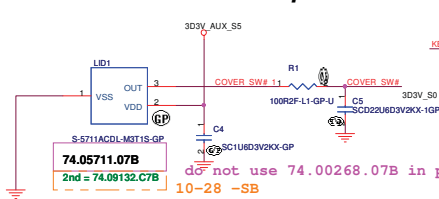
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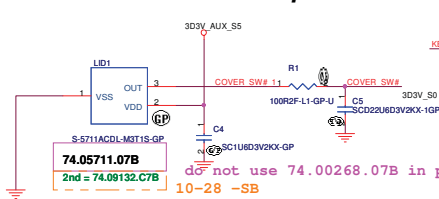
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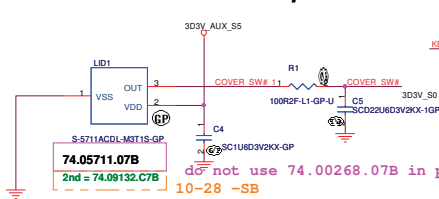
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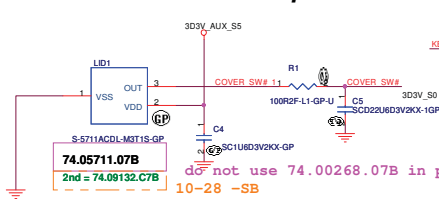
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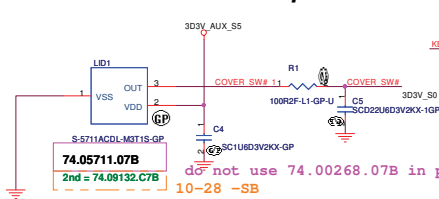
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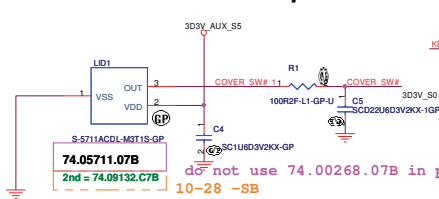
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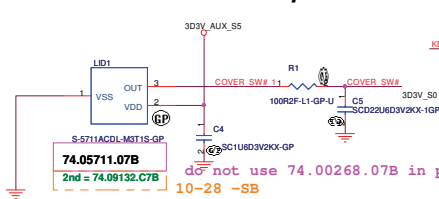
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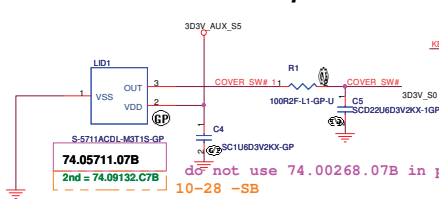
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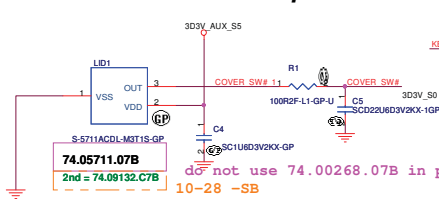
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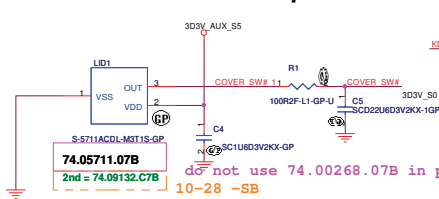
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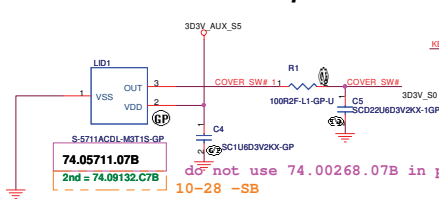
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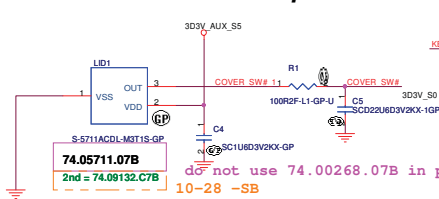
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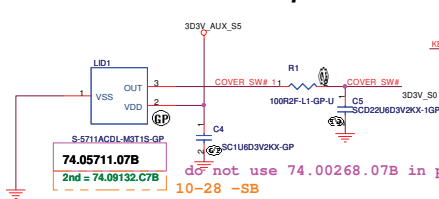
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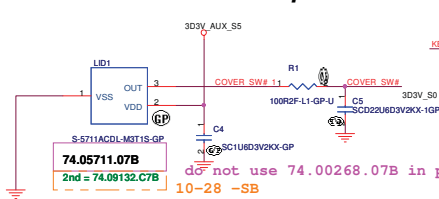
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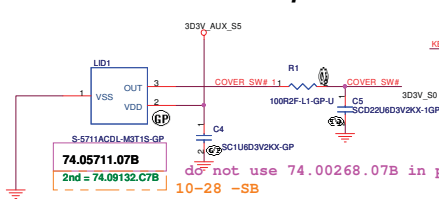
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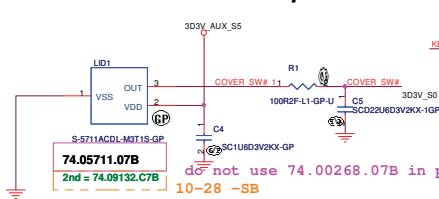
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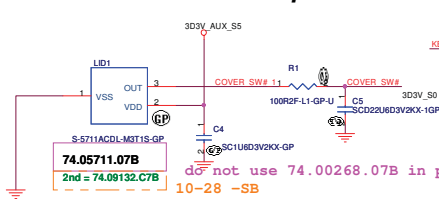
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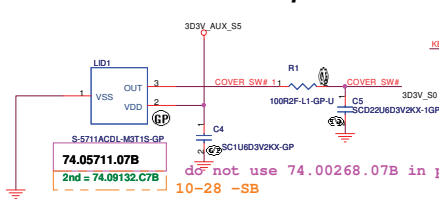
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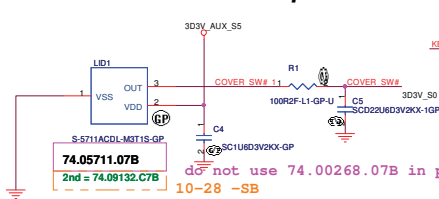
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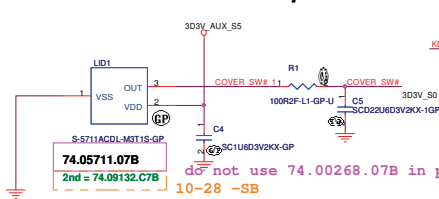
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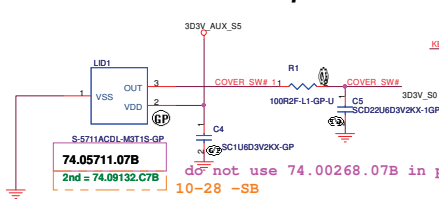
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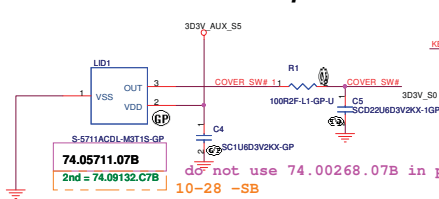
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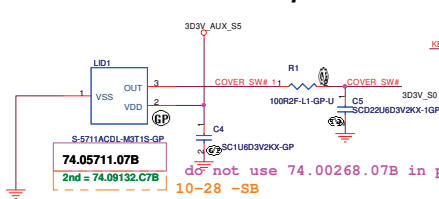
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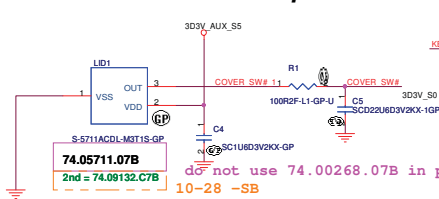
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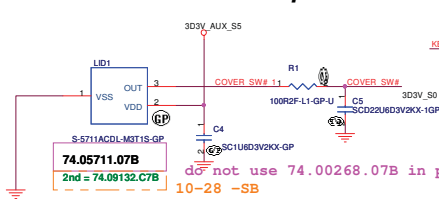
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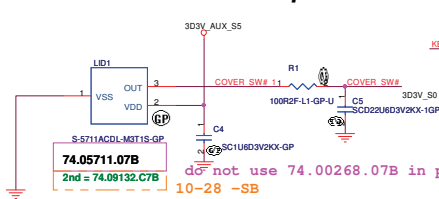
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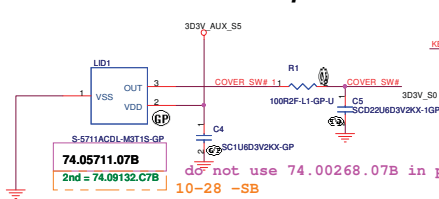
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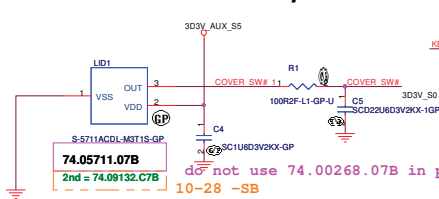
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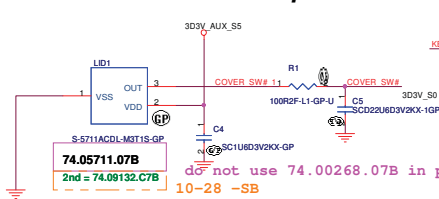
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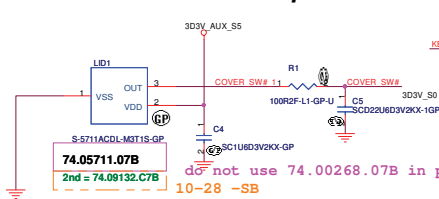
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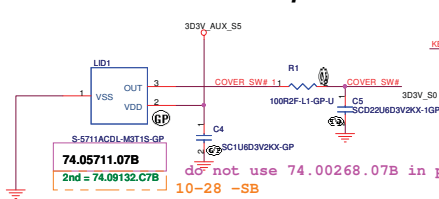
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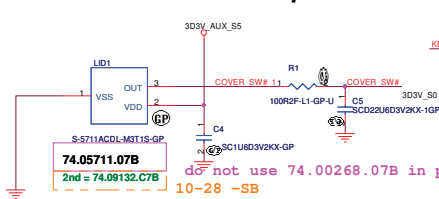
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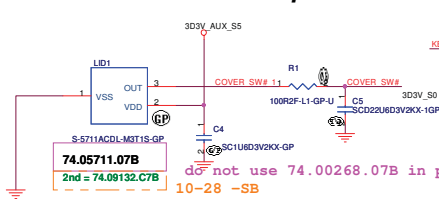
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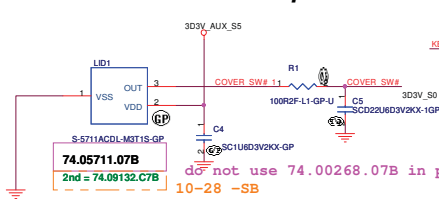
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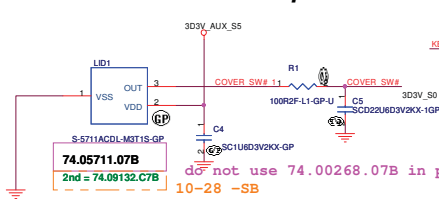
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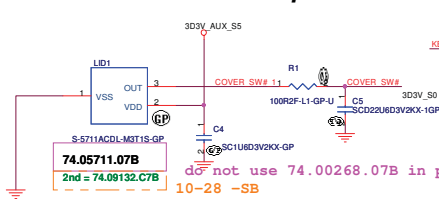
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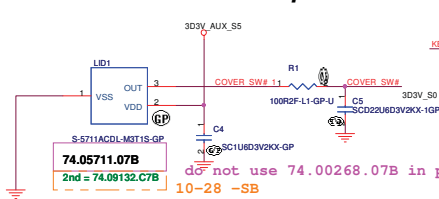
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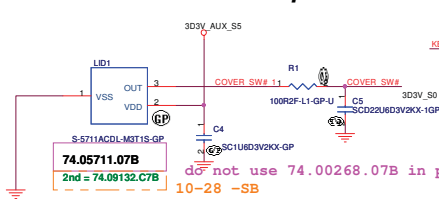
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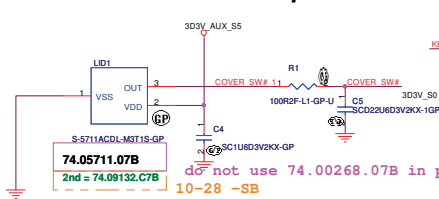
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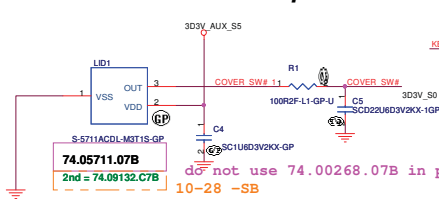
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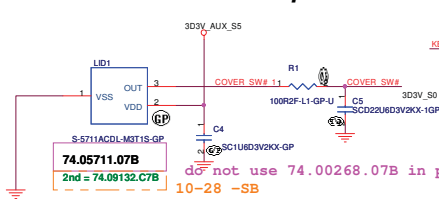
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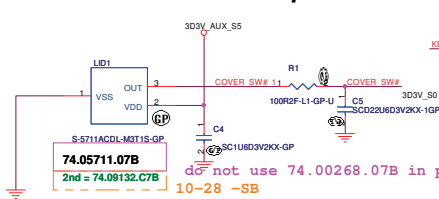
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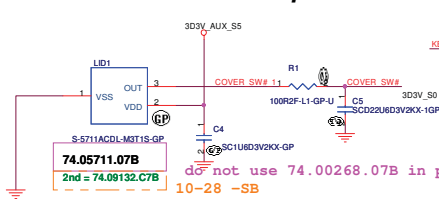
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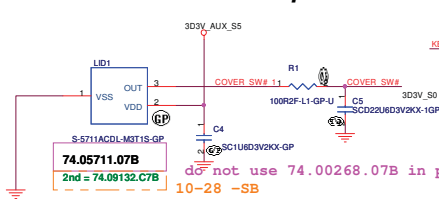
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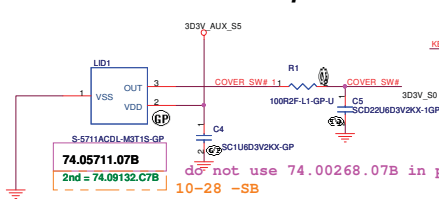
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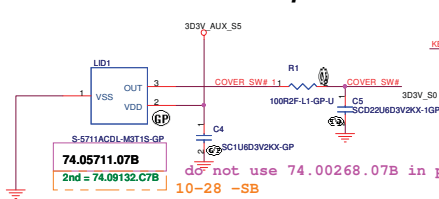
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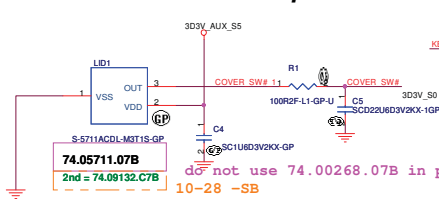
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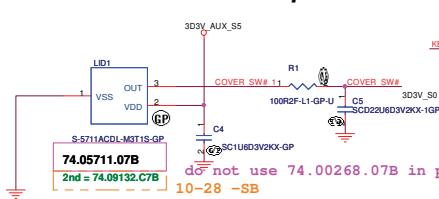
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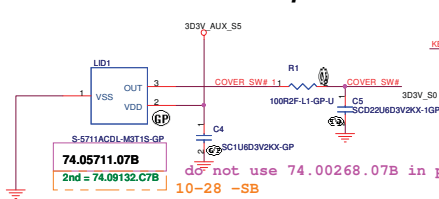
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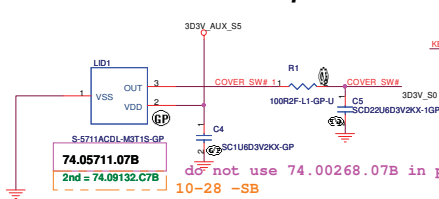
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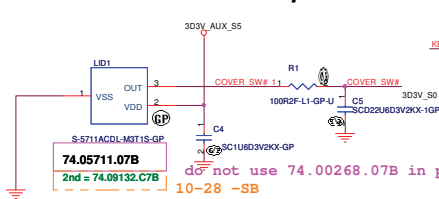
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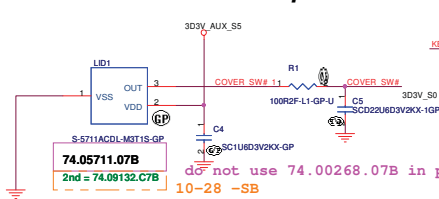
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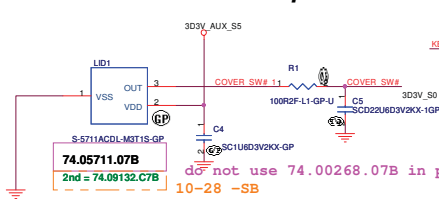
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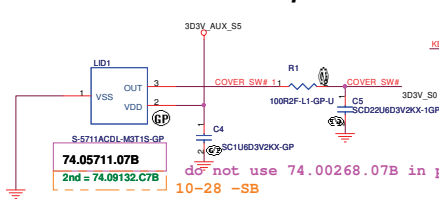
## Cover Up Switch



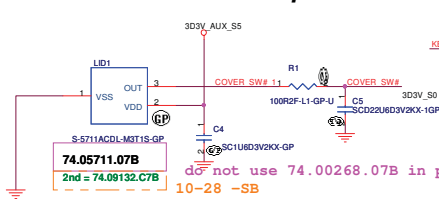
## Cover Up Switch



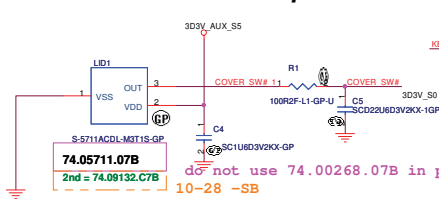
## Cover Up Switch



## Cover Up Switch



## Cover Up Switch



## Cover Up Switch

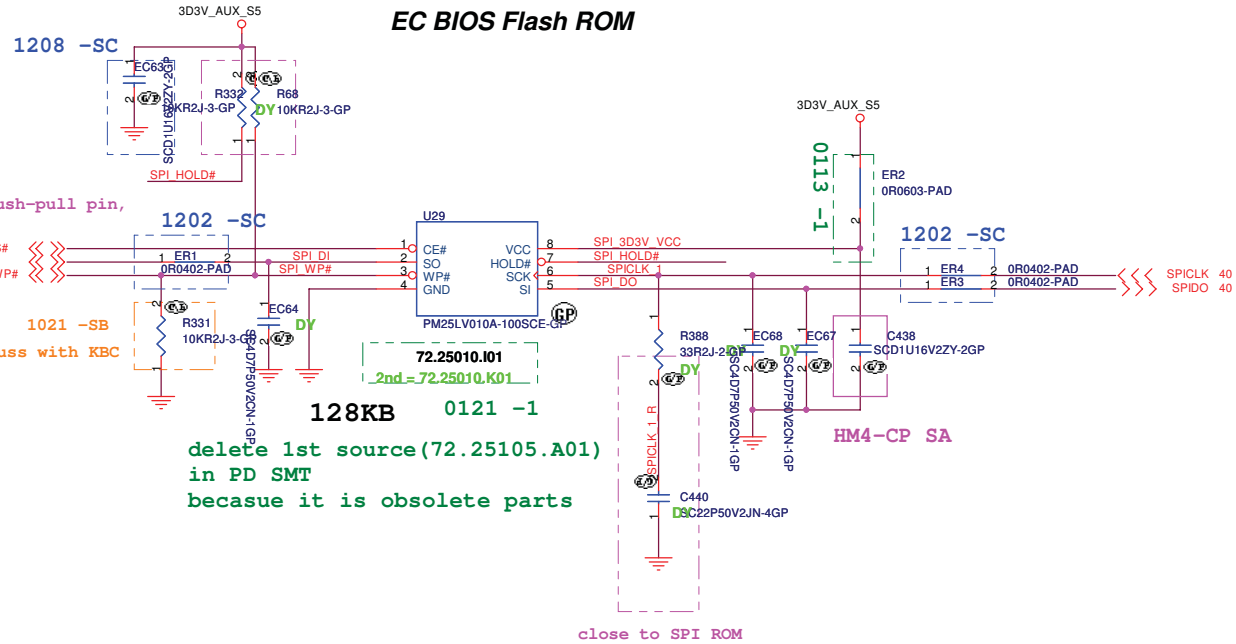
</

for ENE FAE suggest, SPICS# is push-pull pin,  
don't need to pull high

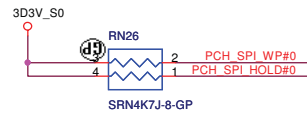
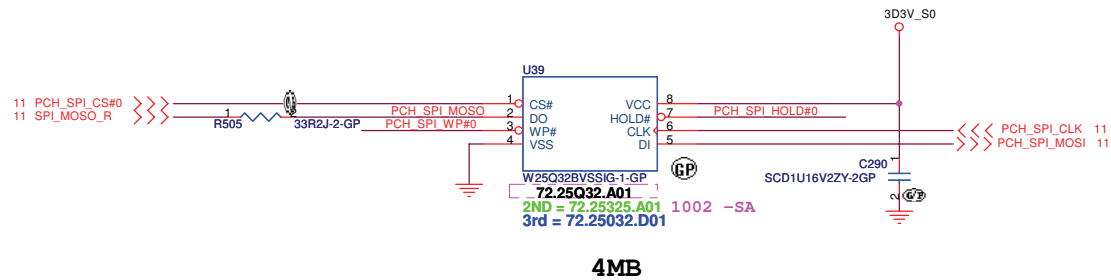
-SA 0930

base on FAE Kevin discuss with KBC

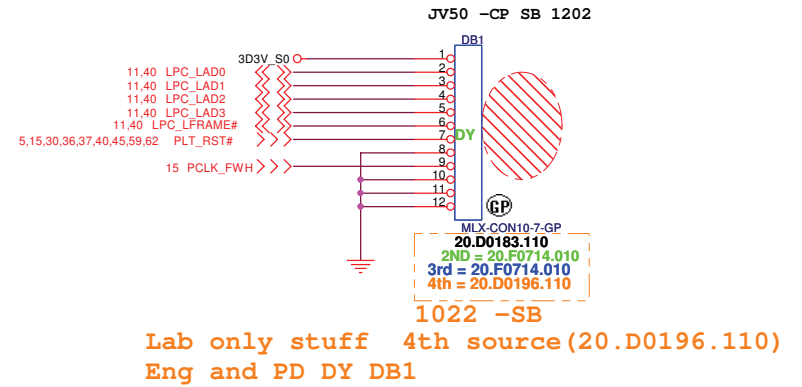
## EC BIOS Flash ROM



## System BIOS Flash ROM



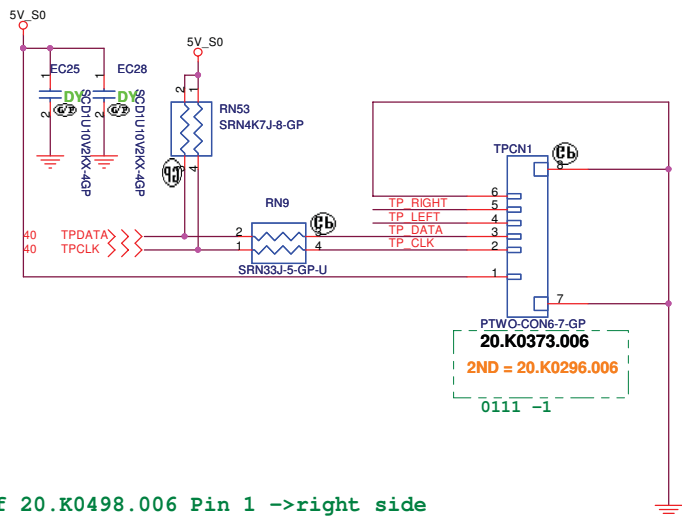
## GOLDEN FINGER FOR DEBUG BOARD



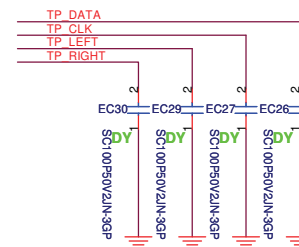
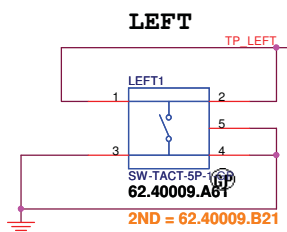
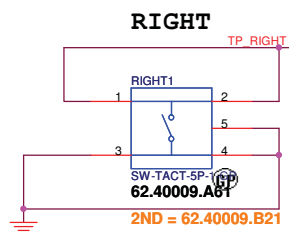
Discrete N11M

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Taipei Hsien 221, Taiwan, R.O.C.

Title		BIOS	
Size	Document Number	HM42-CP	
Date: Friday, January 22, 2010	Sheet 41	of 72	Rev SC

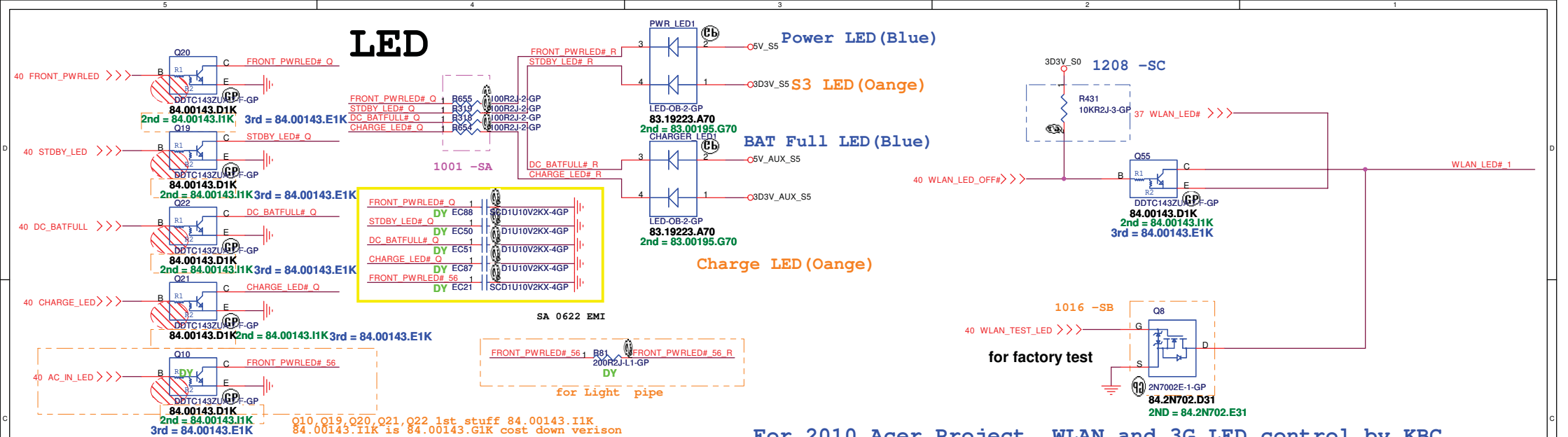


Eng stuff 20.K0498.006 Pin 1 ->right side  
PD change to 20.K0373.006 pin 1 ->left side  
so net mirror Vertically

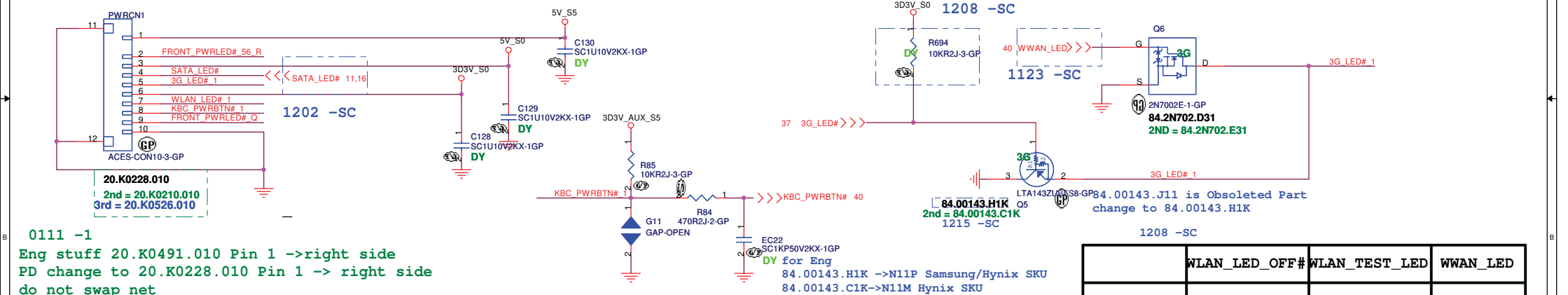


Discrete N11M

# LED



For 2010 Acer Project, WLAN and 3G LED control by KBC



Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

	WLAN_LED_OFF#	WLAN_TEST_LED	WWAN_LED
WLAN ON Always on	L	H	L
WLAN ON (flash)	H	L	L
WWAN_ON	L	L	H
WLAN ON WWAN_ON	L	L	H

### <Core Design>

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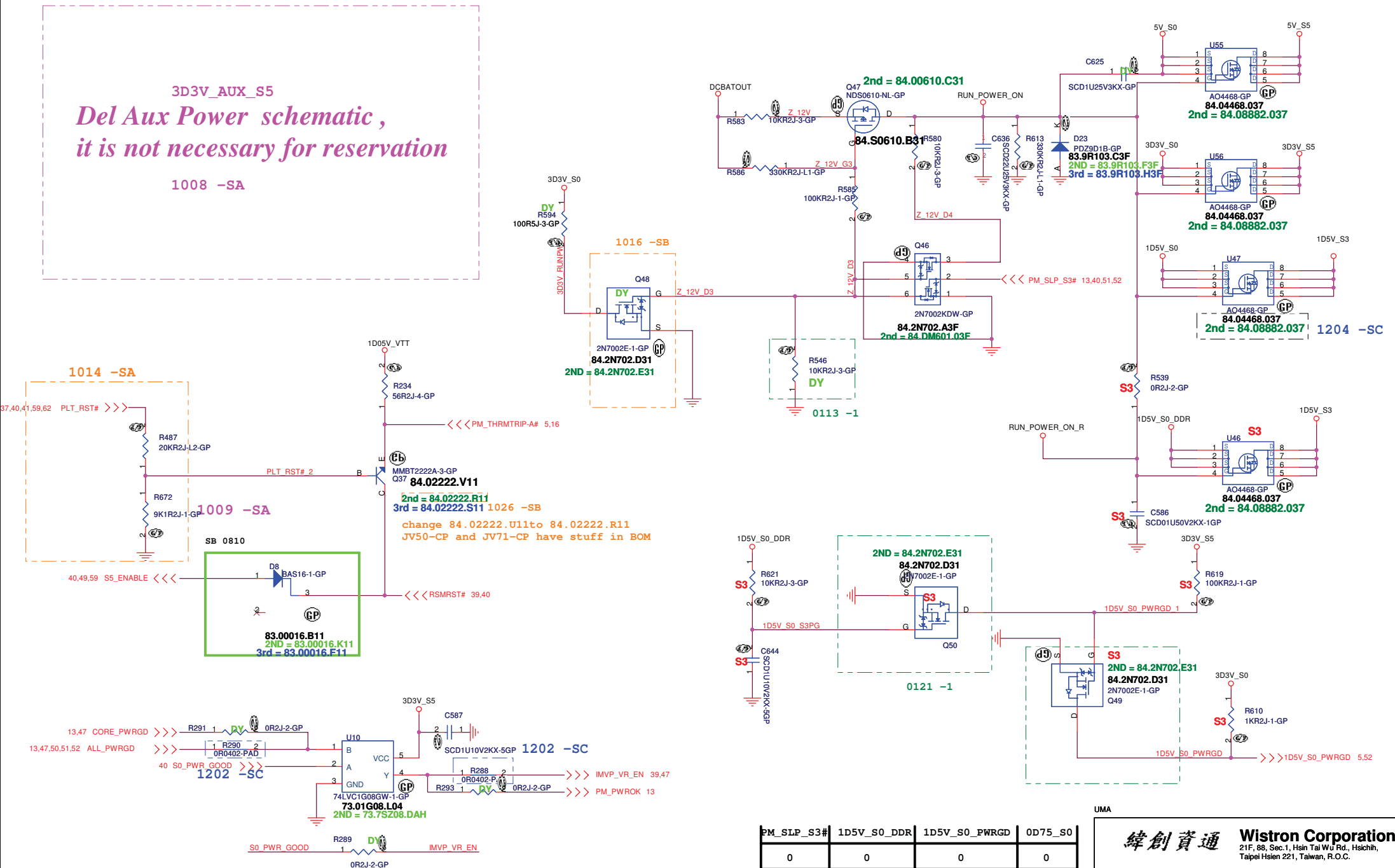
Title			
<b>LED&amp;POWERBD CONN</b>			
Size	Document Number		Rev
	<b>HM42-CP</b>		<b>SO</b>
Date:	Friday, January 22, 2010	Sheet 44 of	72

## Run Power

3D3V\_AUX\_S5

*Del Aux Power schematic ,  
it is not necessary for reservation*

1008 -SA



PM_SLP_S3#	1D5V_S0_DDR	1D5V_S0_PWRGD	0D75_5
0	0	0	0
1	1	1	1

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title	
-------	--

**RUN POWER and 3D3V AUX S5**

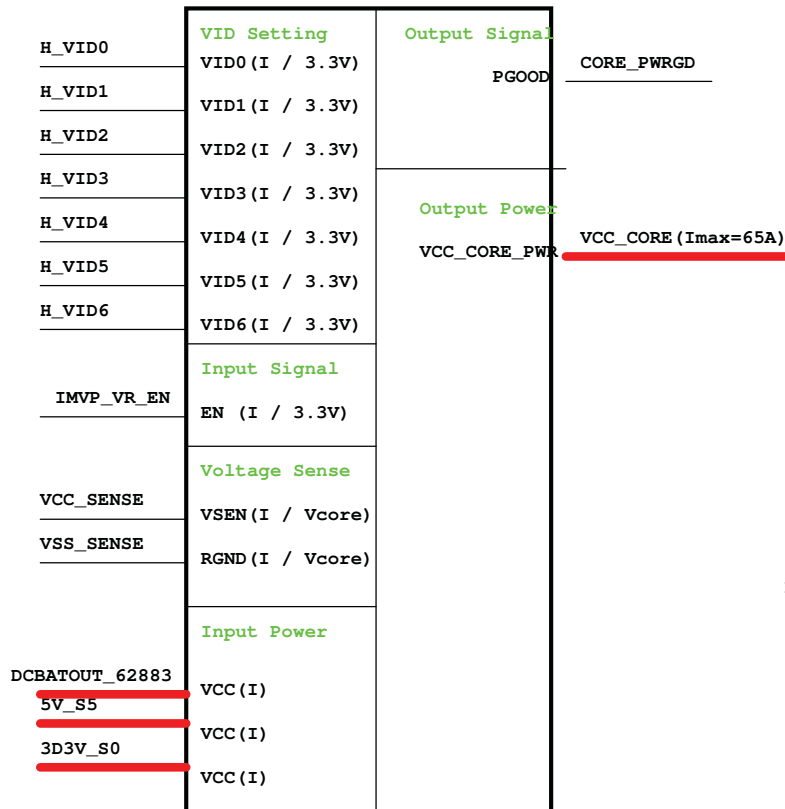
Size	Document Number	Rev
------	-----------------	-----

HM42-CP SC

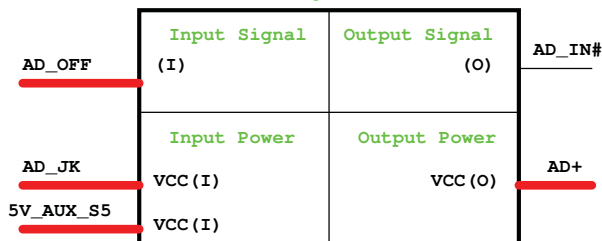
Date: Friday, January 22, 2010 Sheet 45 of 72



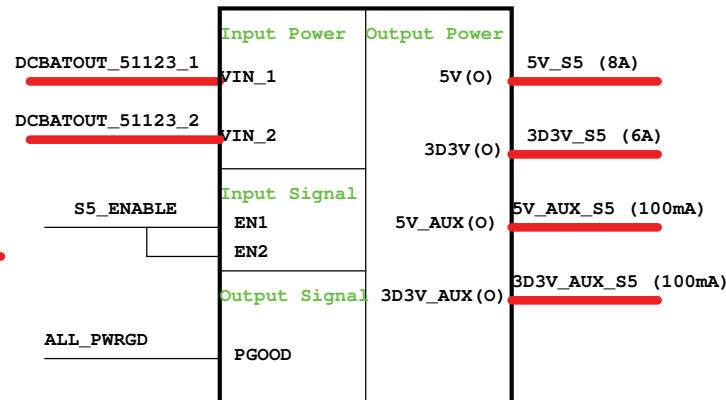
## ISL62883 VCC\_CORE



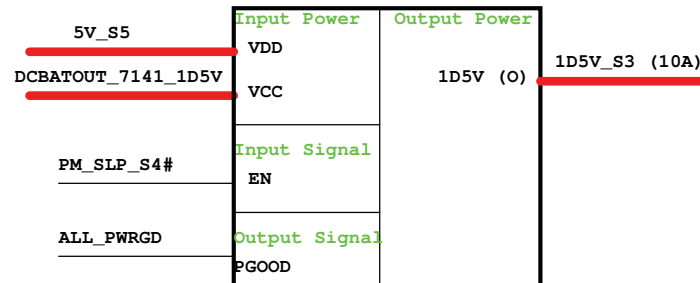
## Adapter



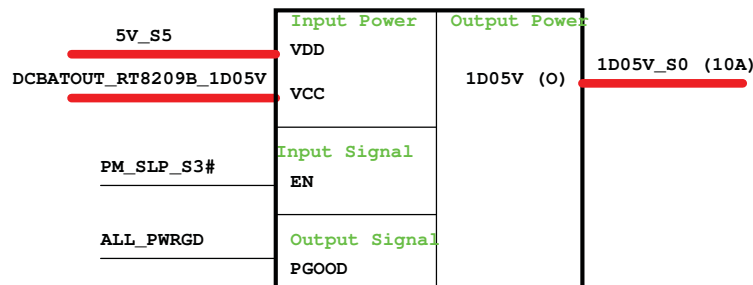
## TPS51123 5V/3D3V



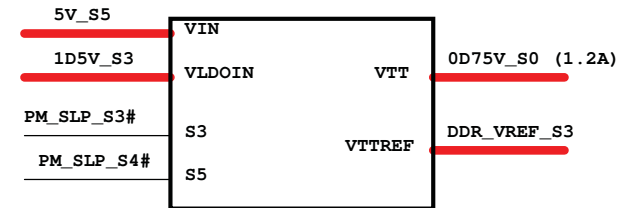
## RT9025 1D5V



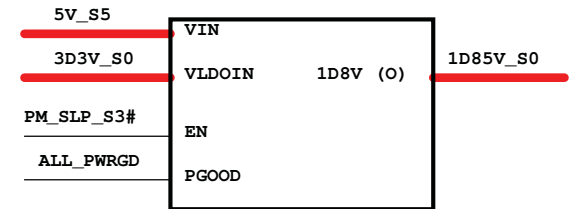
## RT8209B 1D05V



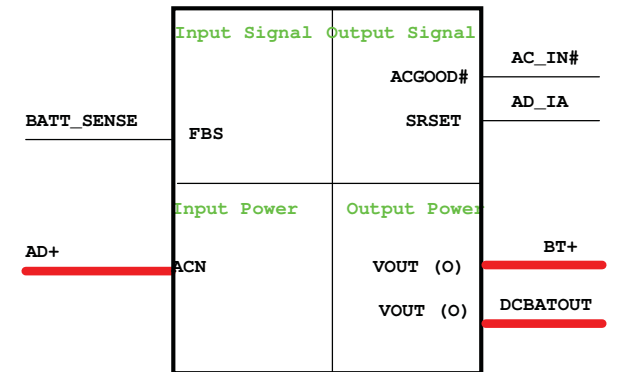
## RT9026 0D75V\_S0



## RT9025 1D8V



## Charger BQ24745



Discrete N11M

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Title

Power Block Diagram

Size

Document Number

Rev

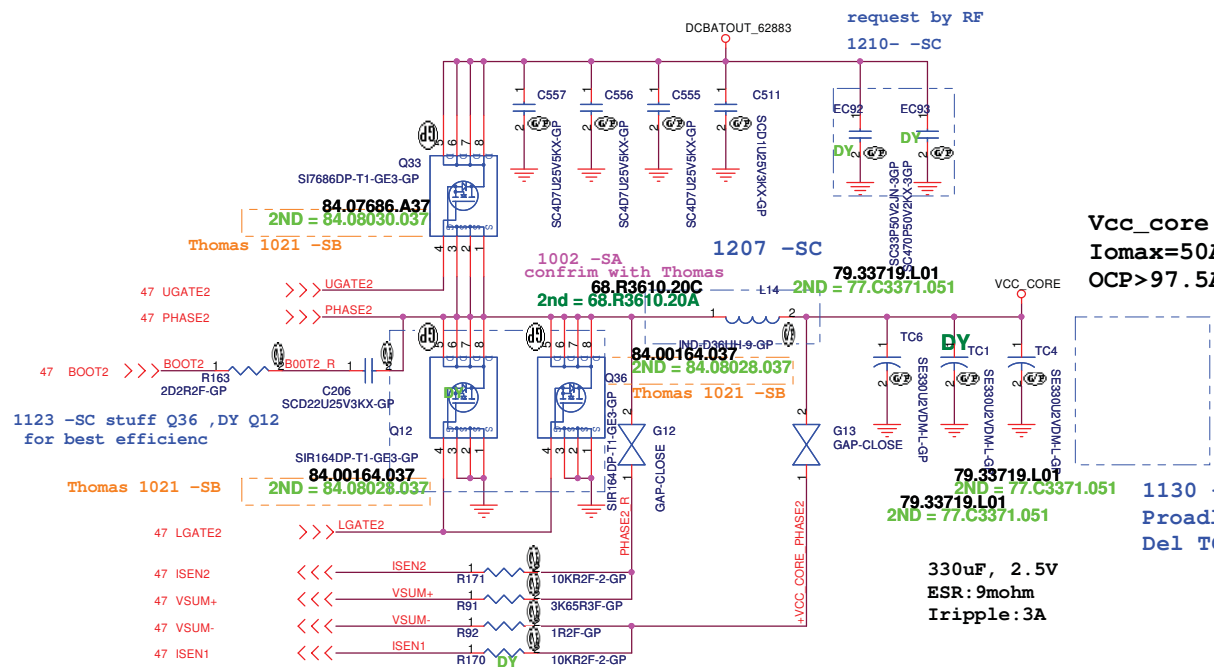
HM42-CP

SC

Date: Friday, January 22, 2010

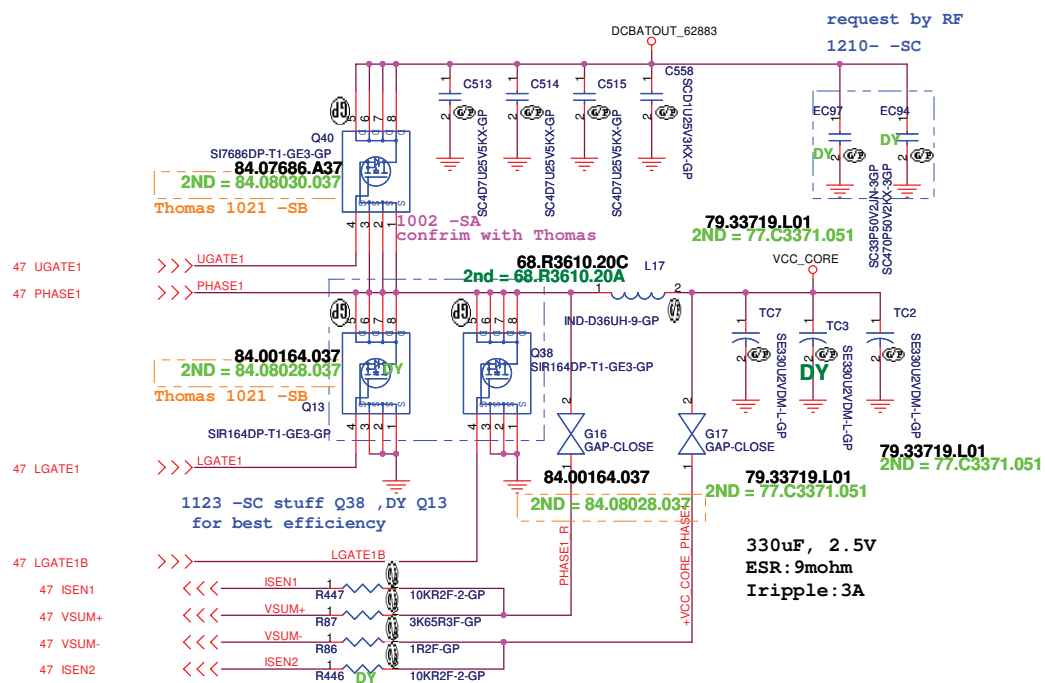
Sheet 46 of 72

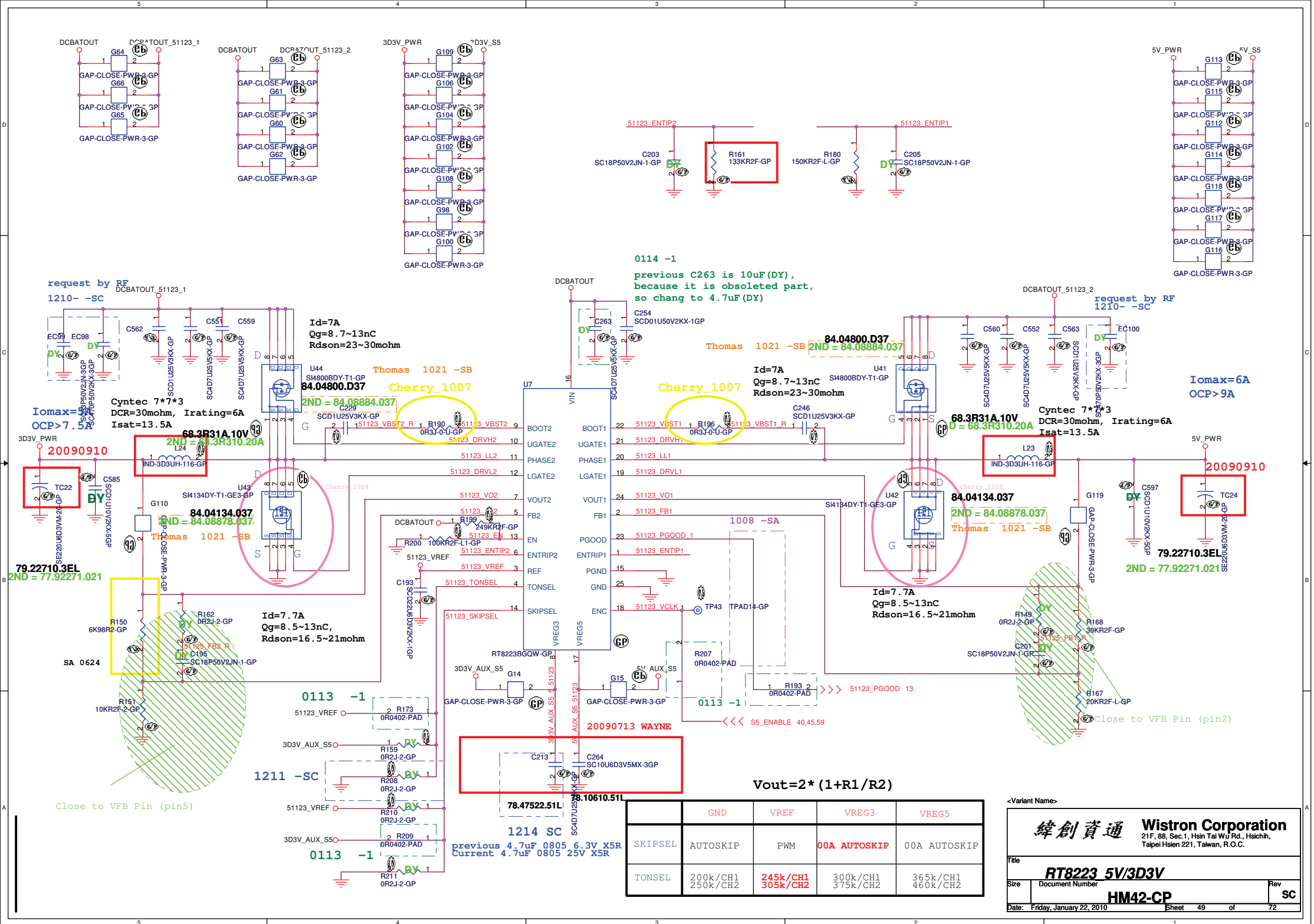




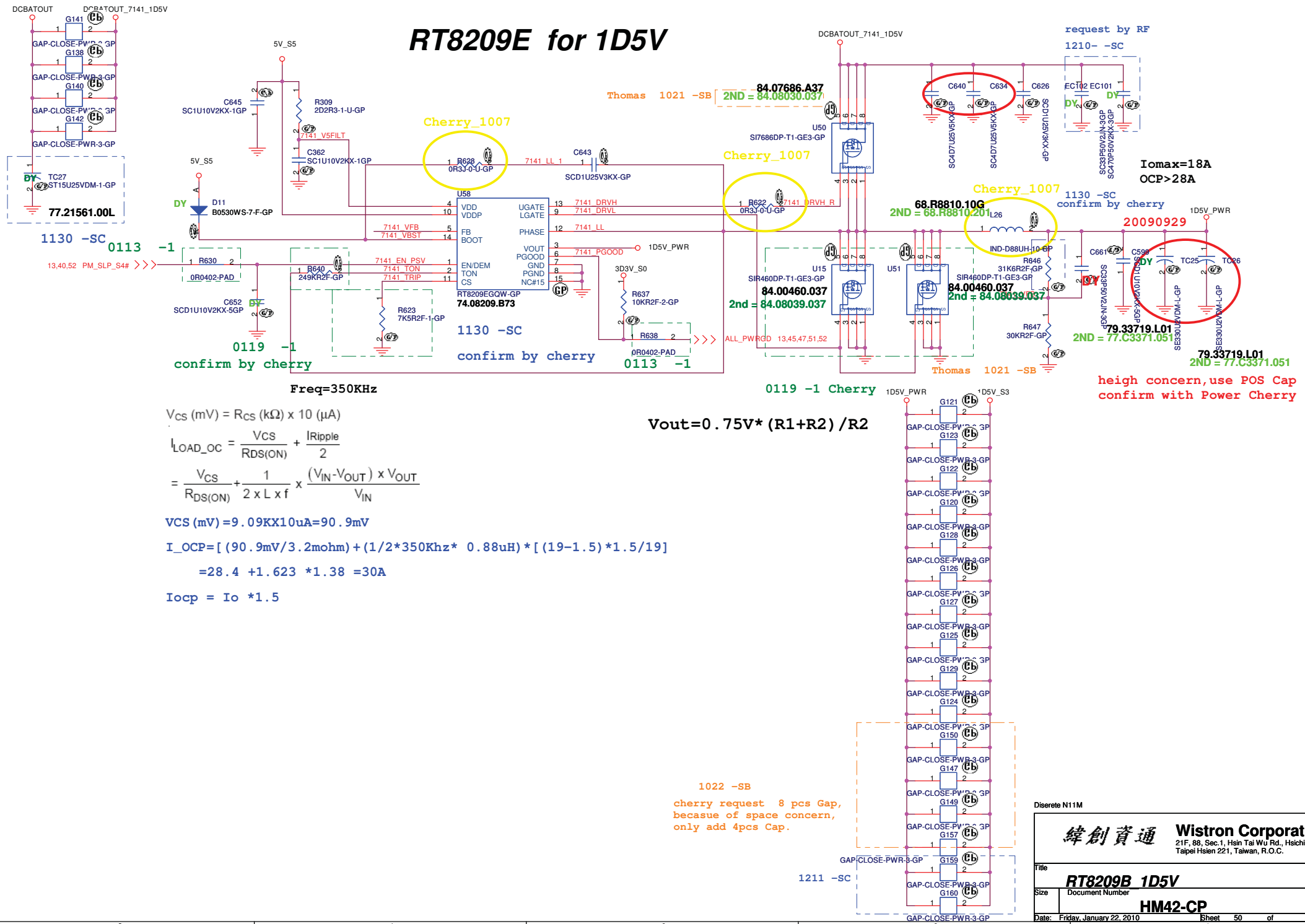
Vcc\_core  
Iomax=50A  
OCP>97.5A

1130 -SC  
Broadlizer Cap power team testing fail,  
Del TC5 for co-layout





## ***RT8209E for 1D5V***



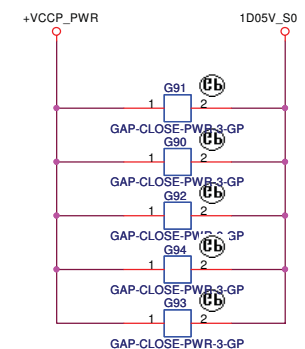
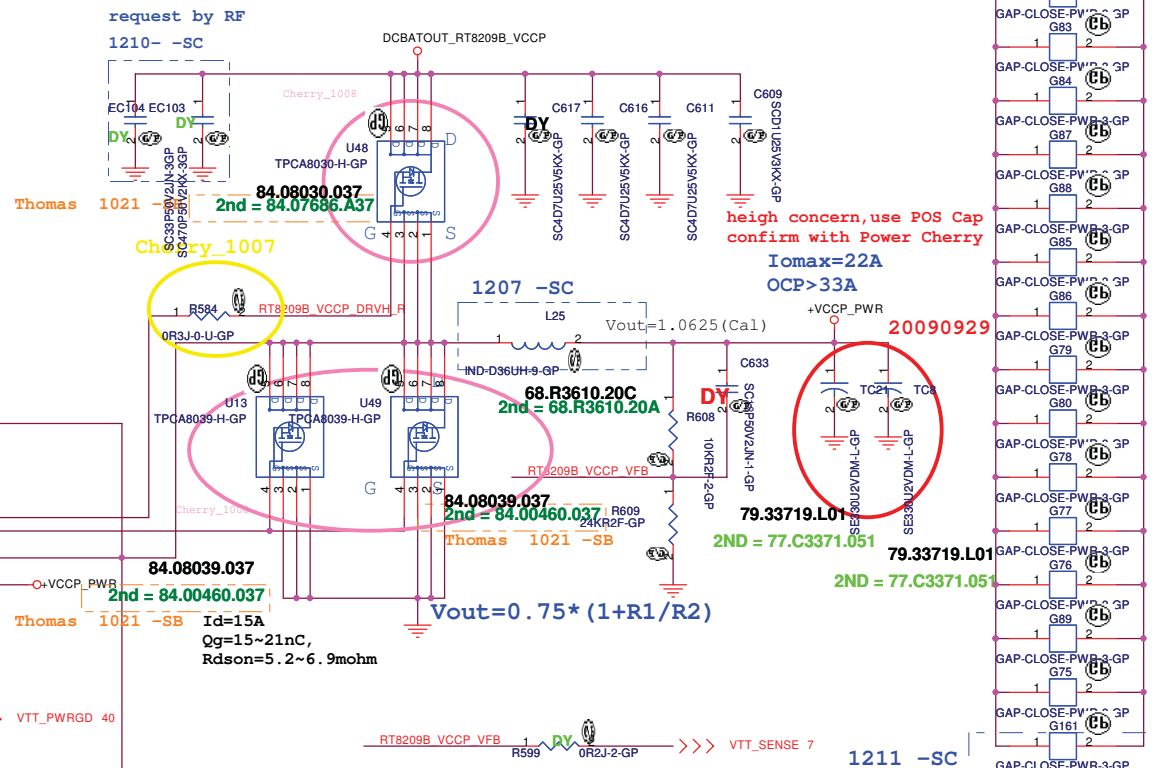
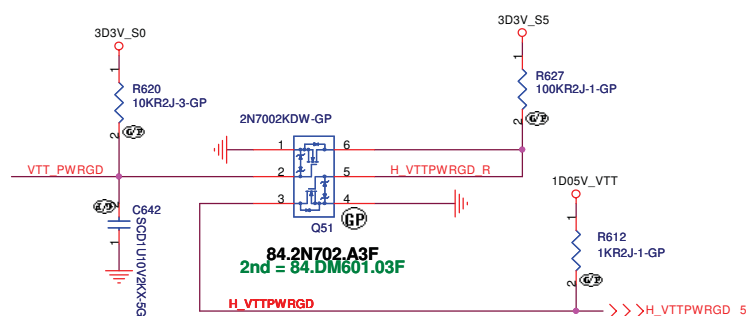
Discrete N11M

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Title			
<b>RT8209B 1D5V</b>			
Size	Document Number		Rev
	<b>HM42-CP</b>		<b>SC</b>
Date:	Friday, January 22, 2010	Sheet 50 of 72	

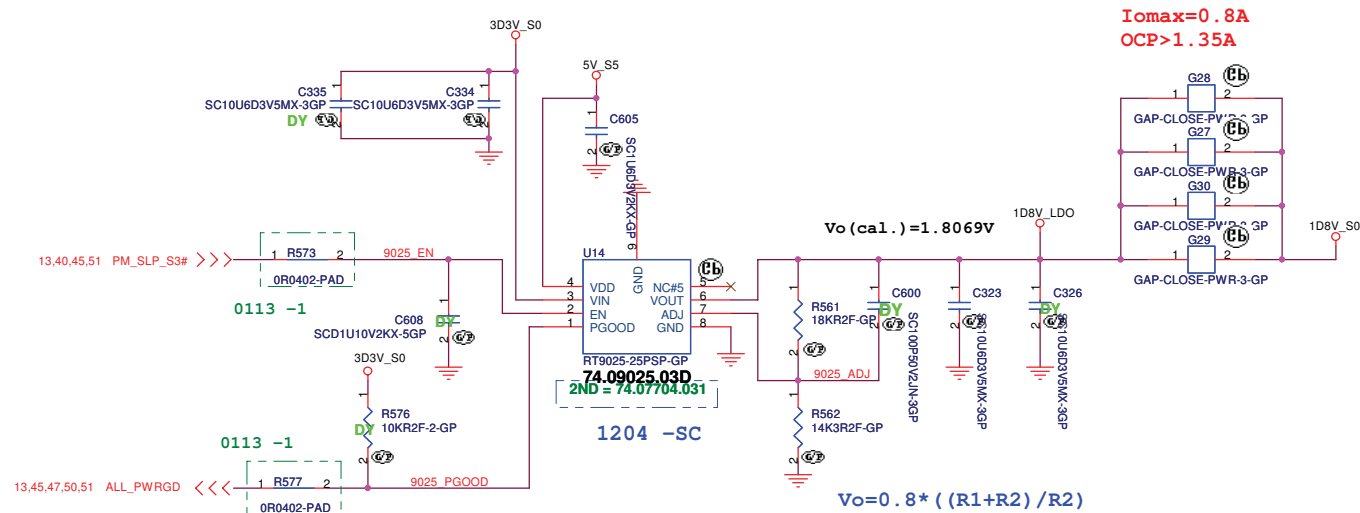


becasue of 1.05V\_S0 and 1.05V\_VTT combin together  
use PM\_SLP\_S3# Enable 1.05V power

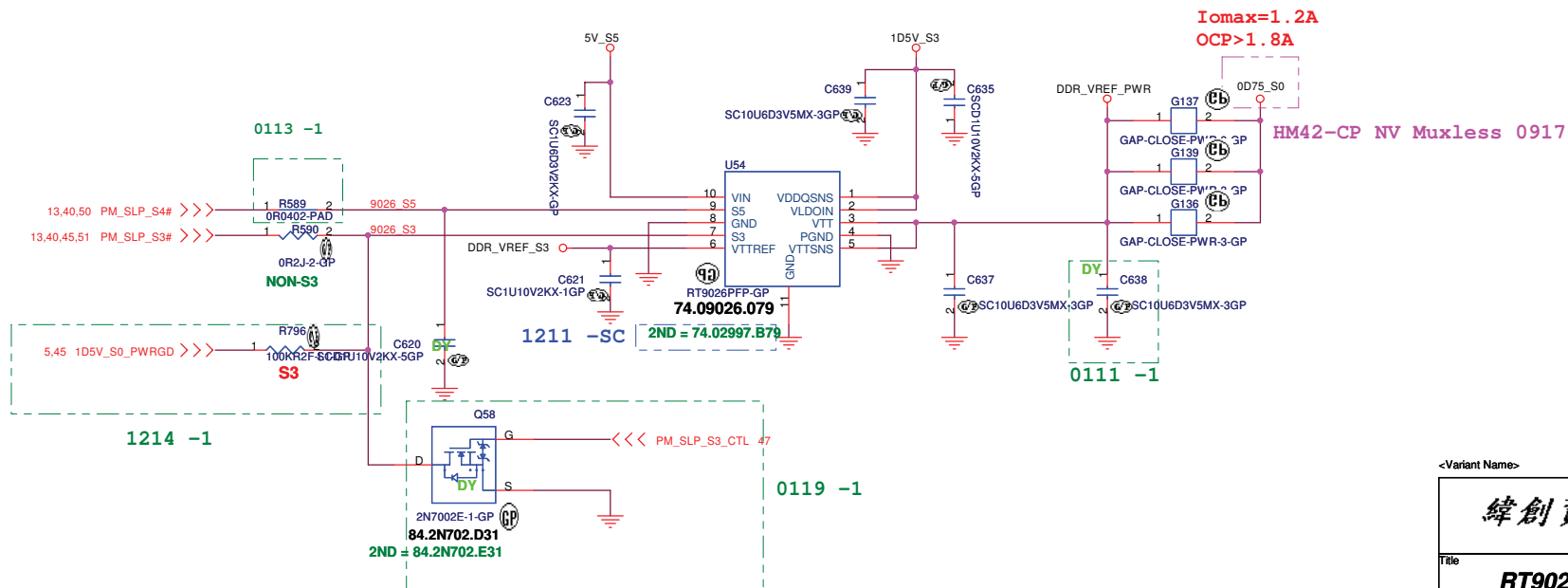


# RT9025 for 1D8V\_S0

20090915



# RT9026 for 0D75V\_S0



<Variant Name>

緯創資通

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Title

**RT9025 1D8V/RT9026 0D75**

Size

Document Number

Rev

**HM42-CP**

SC

Date: Friday, January 22, 2010

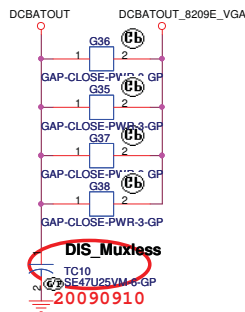
Sheet 52 of 72











## RT8208A for VGA

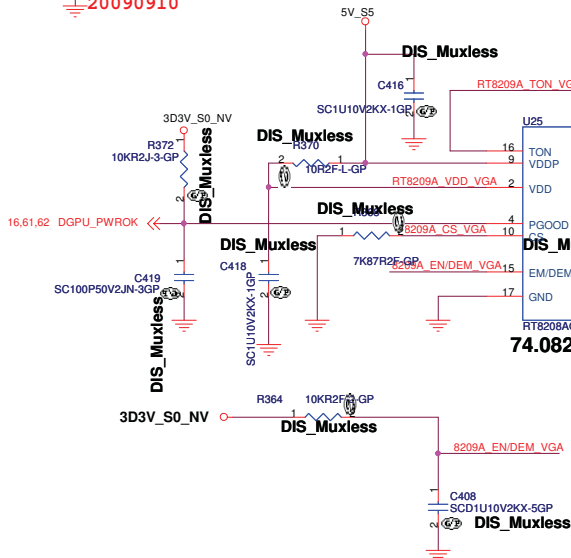


Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVD
Performance (P0)	N11P-GE1	575	790	0.95 V
Performance (P0)	N11P-LP1	475	700	0.85 V
Balanced (P8)	N11P-GE1, N11P-LP1	405	324	0.85 V
Battery (P12)	N11P-GE1, N11P-LP1	135	135	0.80 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVD
Performance (P0)	N11M-GE1	625	790	1.03 V
Performance (P0)	N11M-LP1	525	700	0.86 V
Balanced (P8)	N11M-GE1, N11M-LP1	405	405	0.85 V
Battery (P12)	N11M-GE1, N11M-LP1	135	135	0.85 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVD
Performance (P0)	N11M-OP1	625	790	1.03 V
Performance (P0)	N11M-OP2	525	700	0.86 V
Balanced (P8)	N11M-OP1, N11M-OP2	405	405	0.85 V

**N11P-GE1**  
For 40nm GPU the NVVD and GPIO5 (NVVD\_ALTV0) /GPIO6 (NVVD\_ALTV1) relationship

GPIO6/NVVD_ALTV1	GPIO5/NVVD_ALTV0	NVVD
0	0	0.8
0	1	0.85
1	0	0.95

**N11M-GE1/N11M-OP1**

For 40nm GPU the NVVD and GPIO5 (NVVD\_ALTV0) /GPIO6 (NVVD\_ALTV1) relationship

GPIO6/NVVD_ALTV1	GPIO5/NVVD_ALTV0	NVVD
0	1	0.85
1	0	1.03

RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2//R3)}{(R2//R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2//R4)}{(R2//R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2//R3//R4)}{(R2//R3//R4)} \times 0.75$

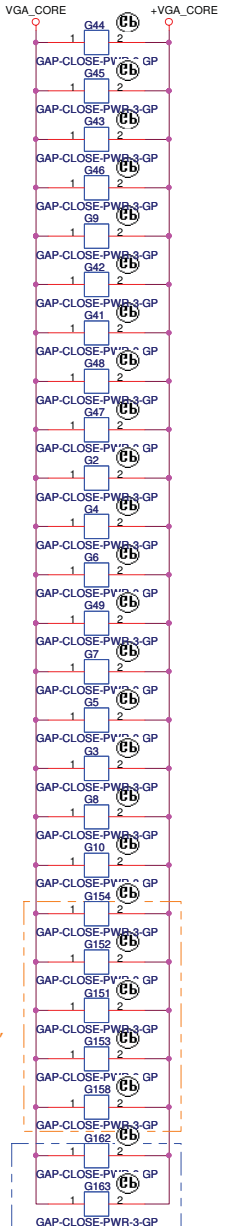
I<sub>max</sub>=27A  
OCP>40A

$$V_{out} = 0.75V * (R1+R2) / R2$$

$$68.3610.20C$$

$$2nd = 68.3610.20A$$

VGA\_CORE



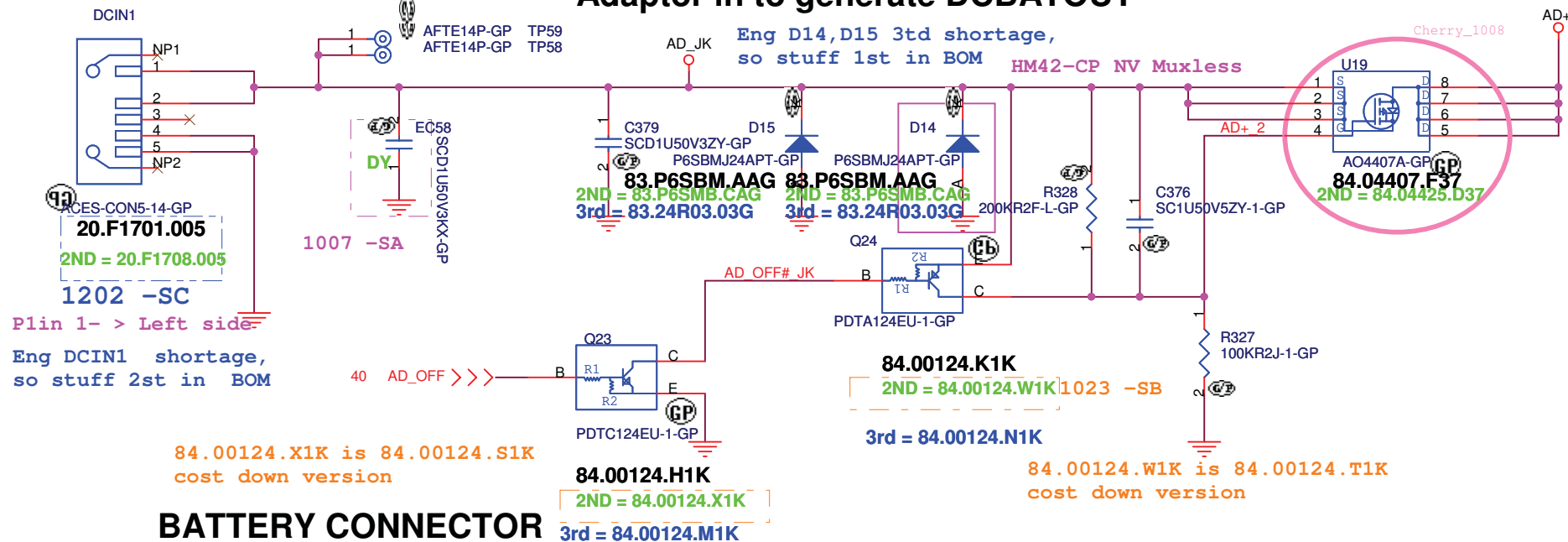
cherry request 9 pcs Gap,  
because of space concern,  
only add 5pcs Cap.

UMA

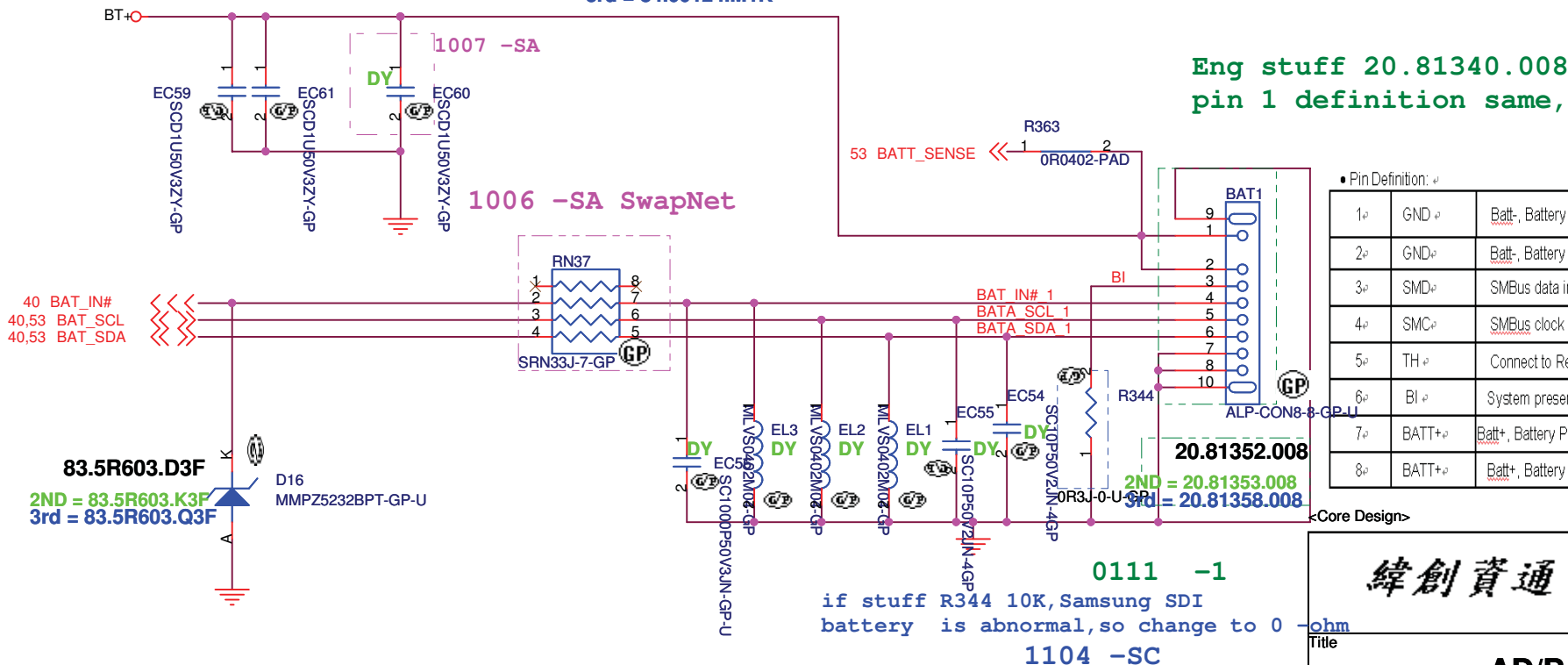
緯創資通 Wistron Corporation  
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Size	Document Number	Rev
Custom	HM42-CP	
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## Adaptor in to generate DCBATOUT



## BATTERY CONNECTOR



- Pin Definition:  $\leftarrow$

1 <sup>o</sup>	GND <sup>o</sup>	Batt-, Battery Negative Terminal <sup>o</sup>
2 <sup>o</sup>	GND <sup>o</sup>	Batt-, Battery Negative Terminal <sup>o</sup>
3 <sup>o</sup>	SMD <sup>o</sup>	SMBus data interface I/O pin <sup>o</sup>
4 <sup>o</sup>	SMC <sup>o</sup>	SMBus clock interface I/O pin <sup>o</sup>
5 <sup>o</sup>	TH <sup>o</sup>	Connect to Resistor to GND (10kΩ to GND) <sup>o</sup>
6 <sup>o</sup>	BI <sup>o</sup>	System present pin, low active <sup>o</sup>
7 <sup>o</sup>	BATT+ <sup>o</sup>	Batt+, Battery Positive Terminal <sup>o</sup>
8 <sup>o</sup>	BATT+ <sup>o</sup>	Batt+, Battery Positive Terminal <sup>o</sup>

## <Core Design>

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Title

## AD/BATT CONN

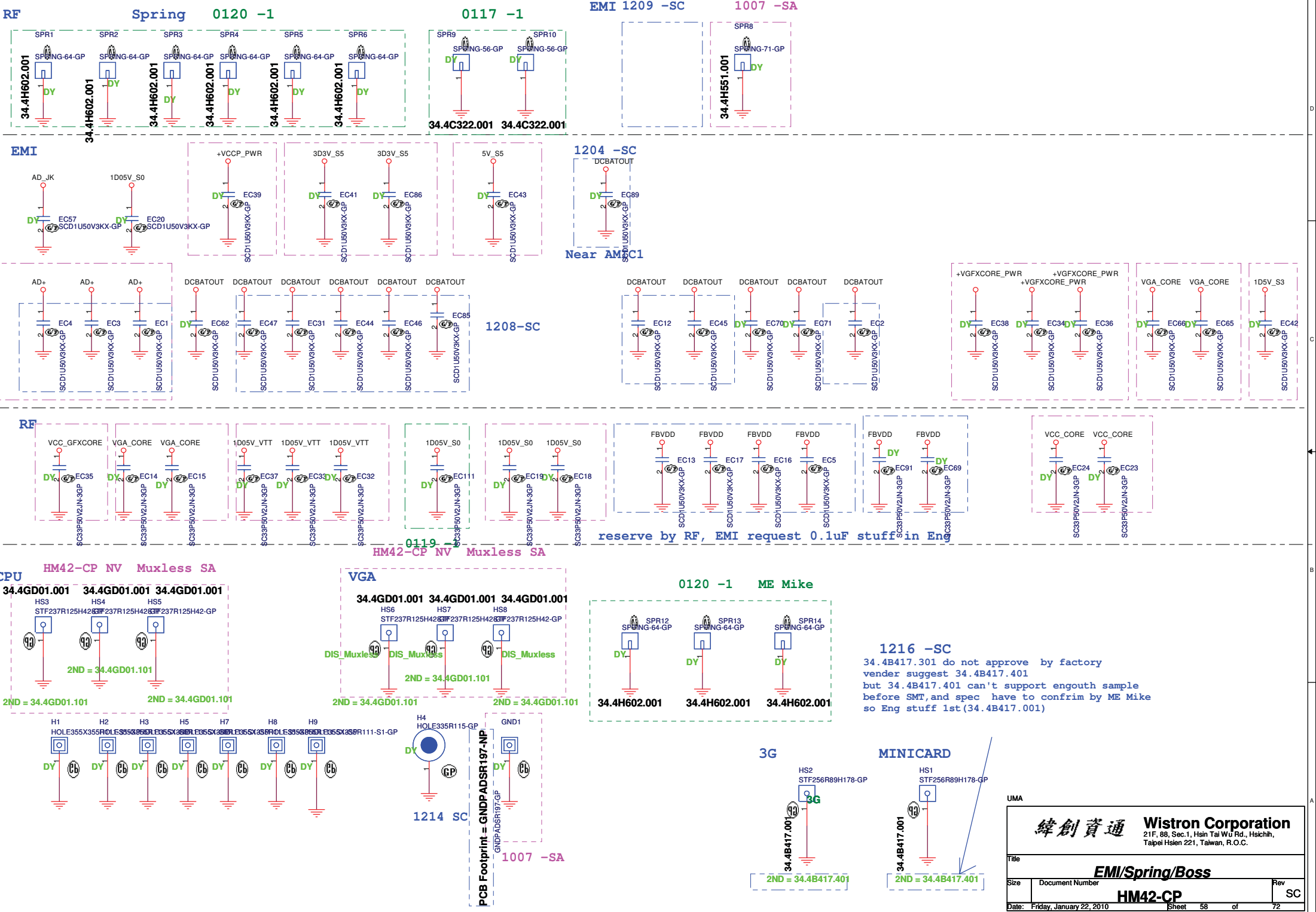
## HM42-CP

SC

Date: Friday, January 22, 2010

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## Check test point

~~delete 3D3V\_S0 test point~~



Test Point放在Dimm Door打開可量測處

<Variant Name>

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Title

**AFTE TP**

Size

Document Number

**HM42-CP**

Rev

**SC**

Date: Friday, January 22, 2010

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**+3VS to 1.8V Transfer**

**+1.5V to FBVDD Transfer**

**+1.05V to +1.05V\_NV Transfer**

**Discharge Circuit**

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**HM42-CP**

**Rev SC**

**Date: Friday, January 22, 2010**

**Sheet 61 of 72**

**+3VS to 1.8V Transfer**

**+1.5V to FBVDD Transfer**

**+1.05V to +1.05V\_NV Transfer**

**Discharge Circuit**

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**HM42-CP**

**Rev SC**

**Date: Friday, January 22, 2010**

**Sheet 61 of 72**

**+3VS to 1.8V Transfer**

**+1.5V to FBVDD Transfer**

**+1.05V to +1.05V\_NV Transfer**

**Discharge Circuit**

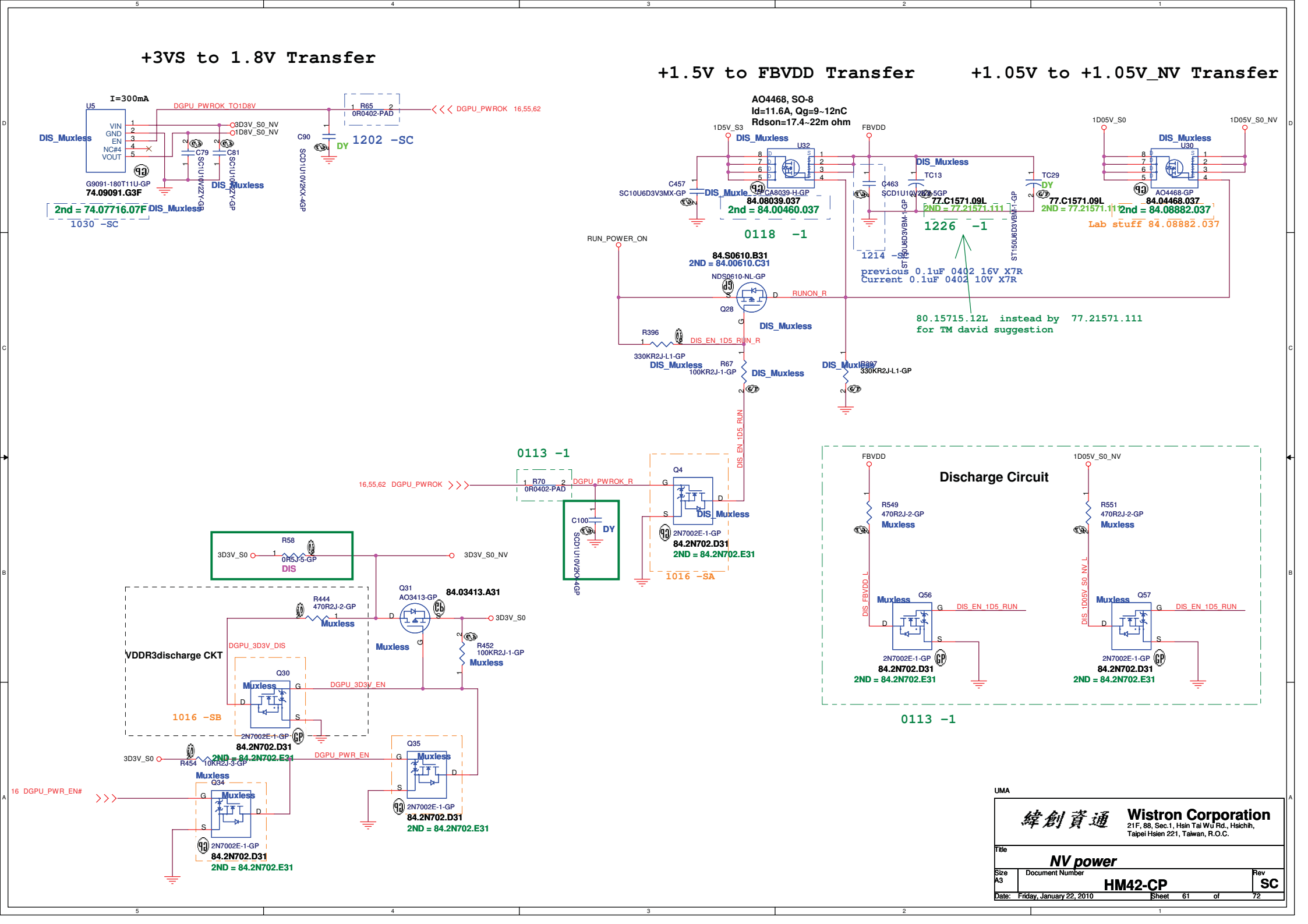
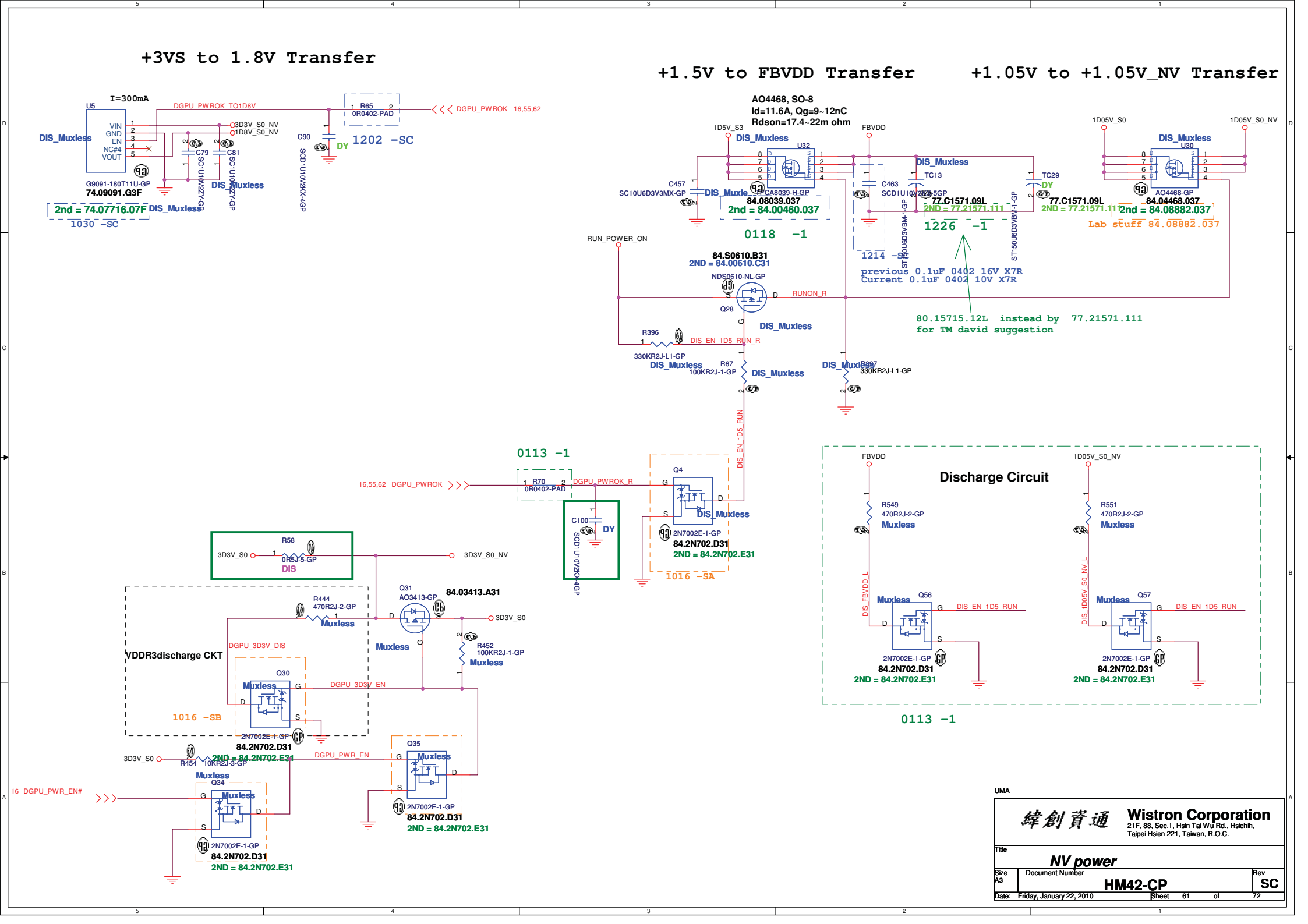
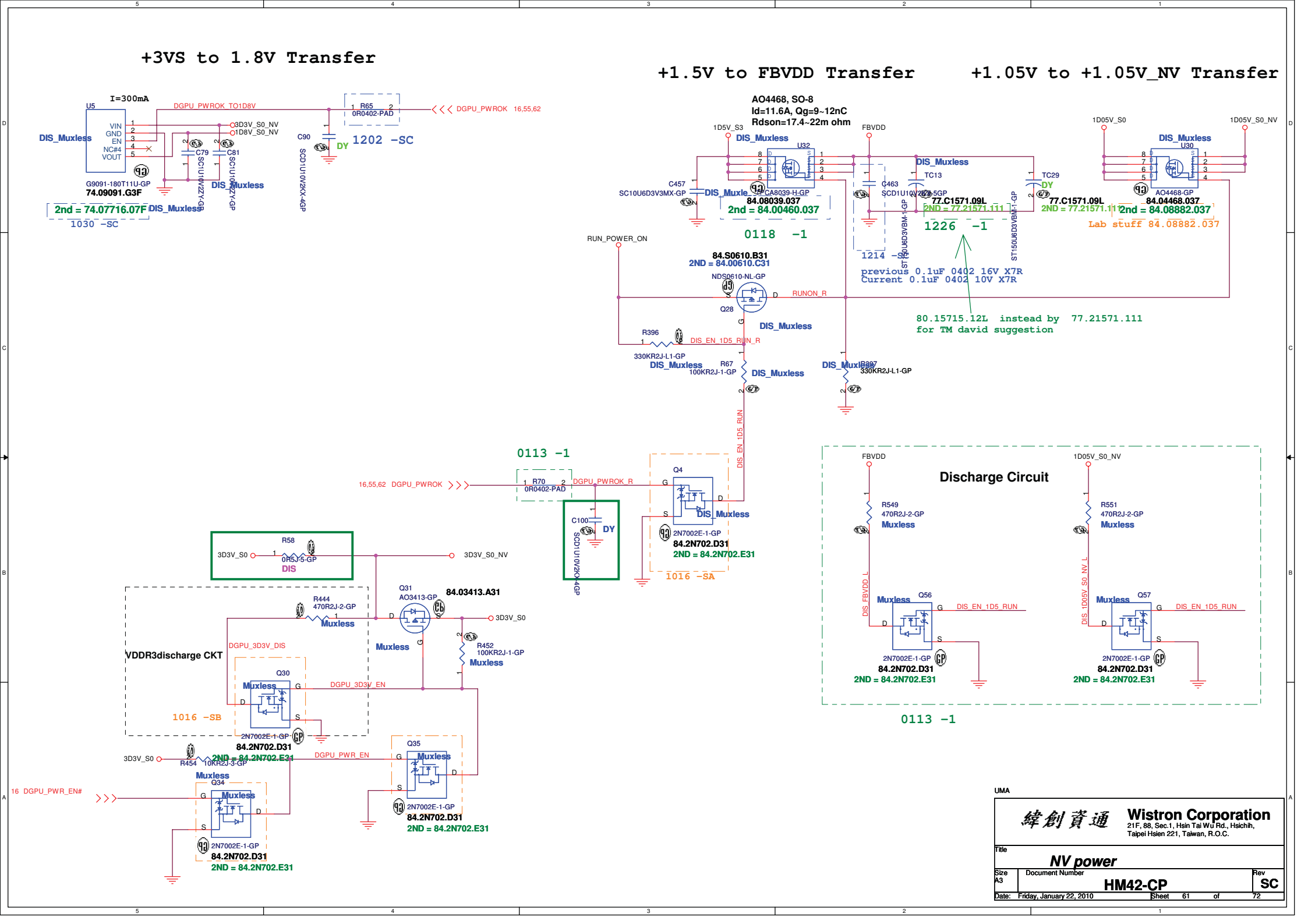
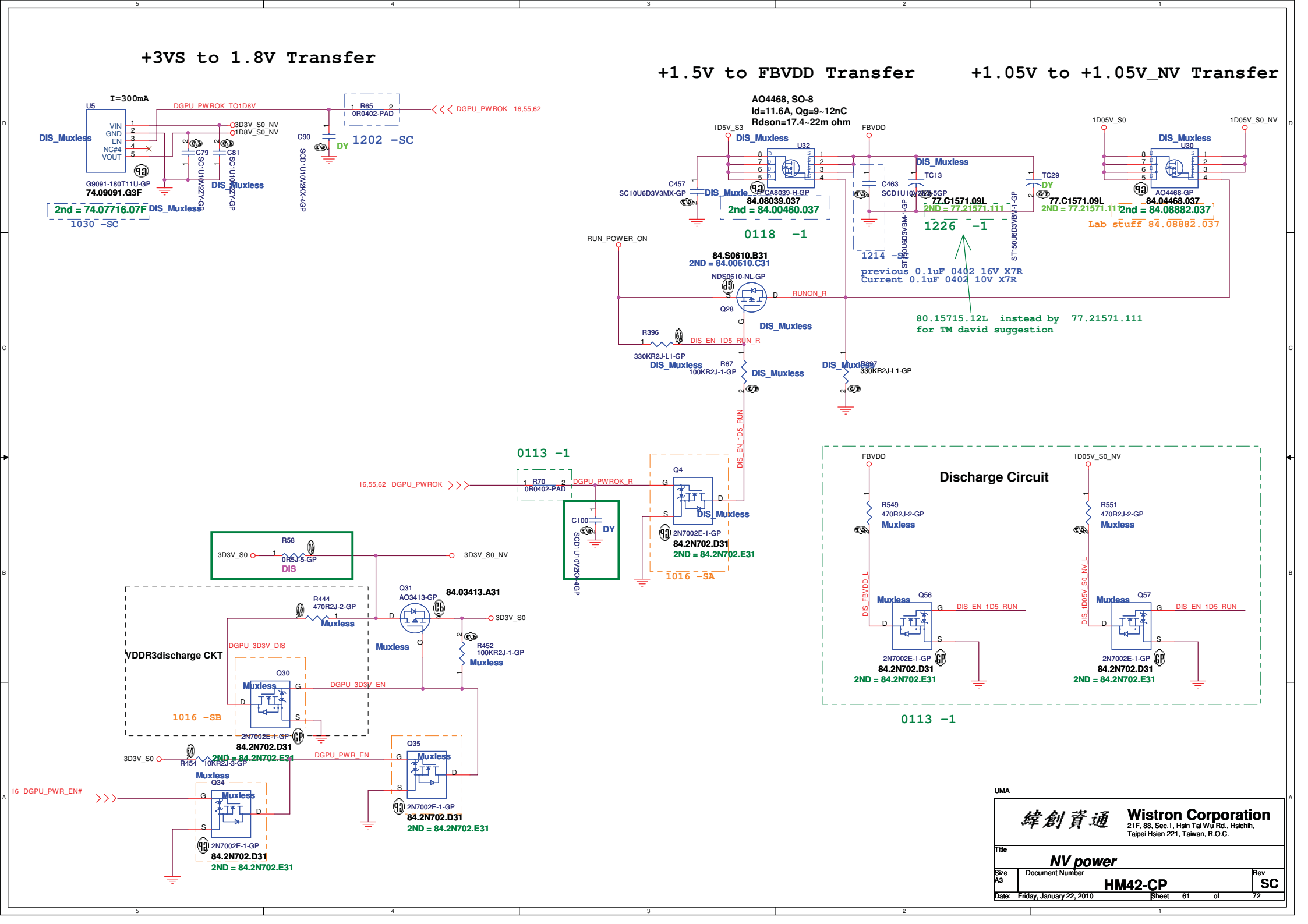
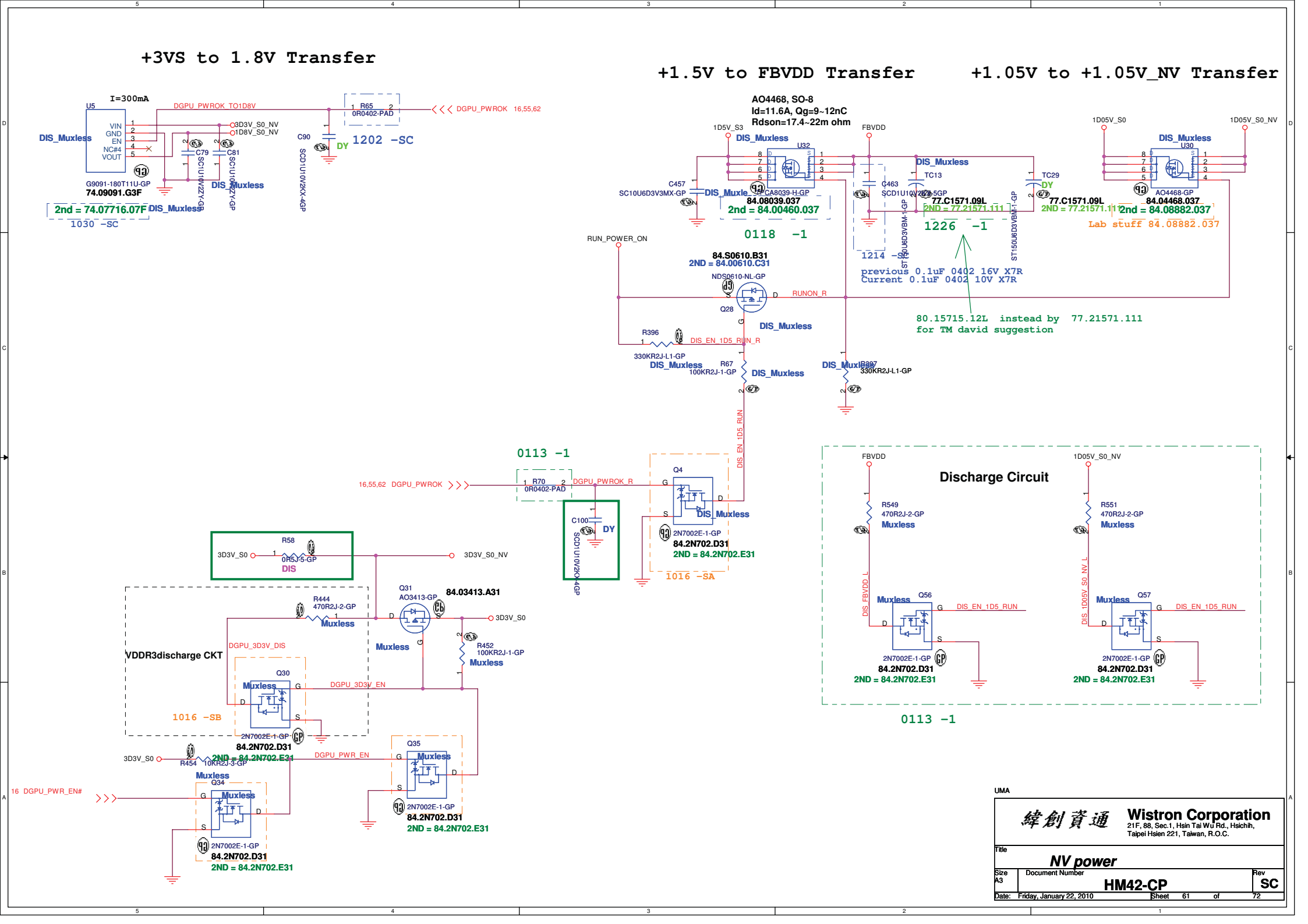
**Wistron Corporation**  
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**HM42-CP**

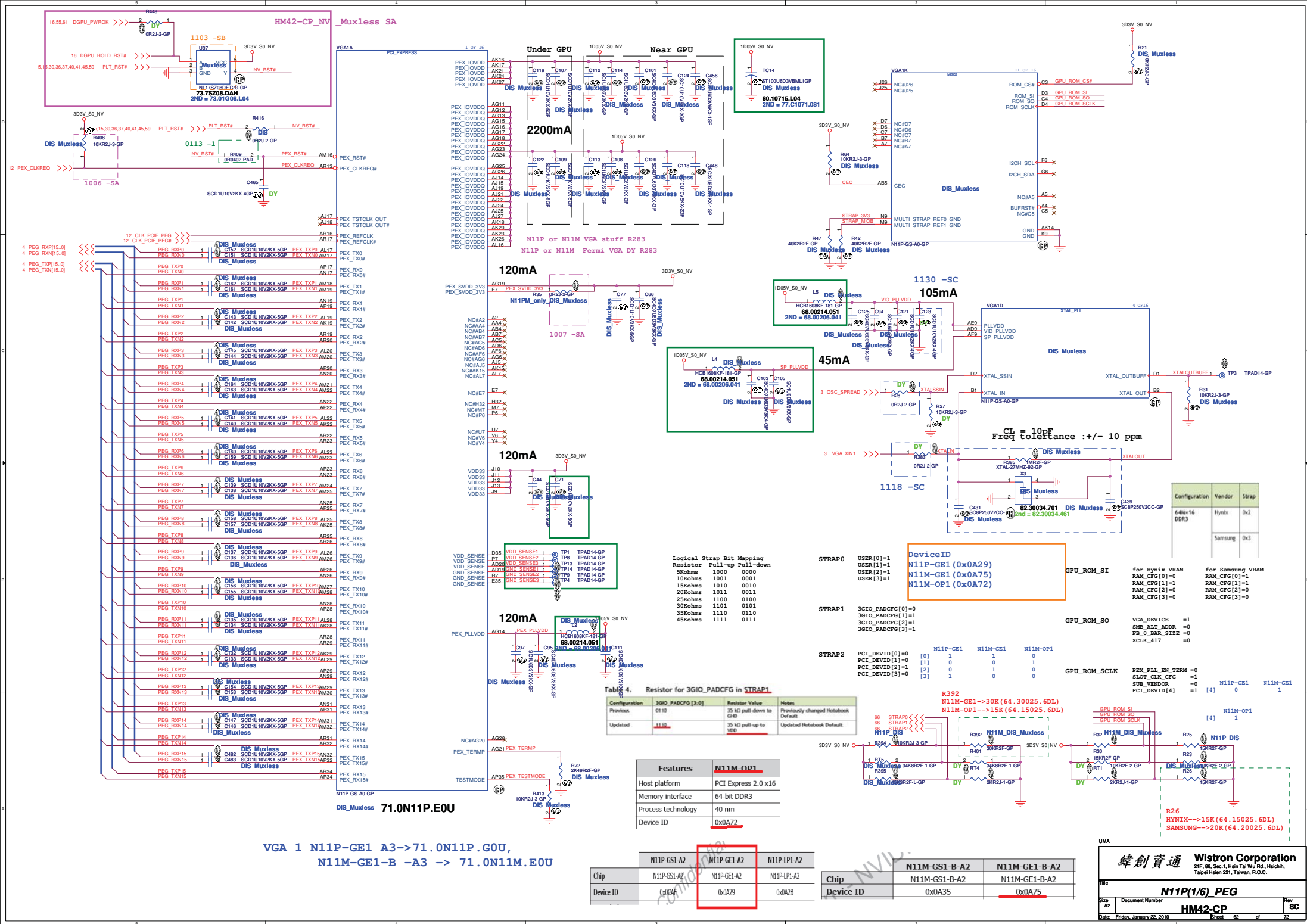
**Rev SC**

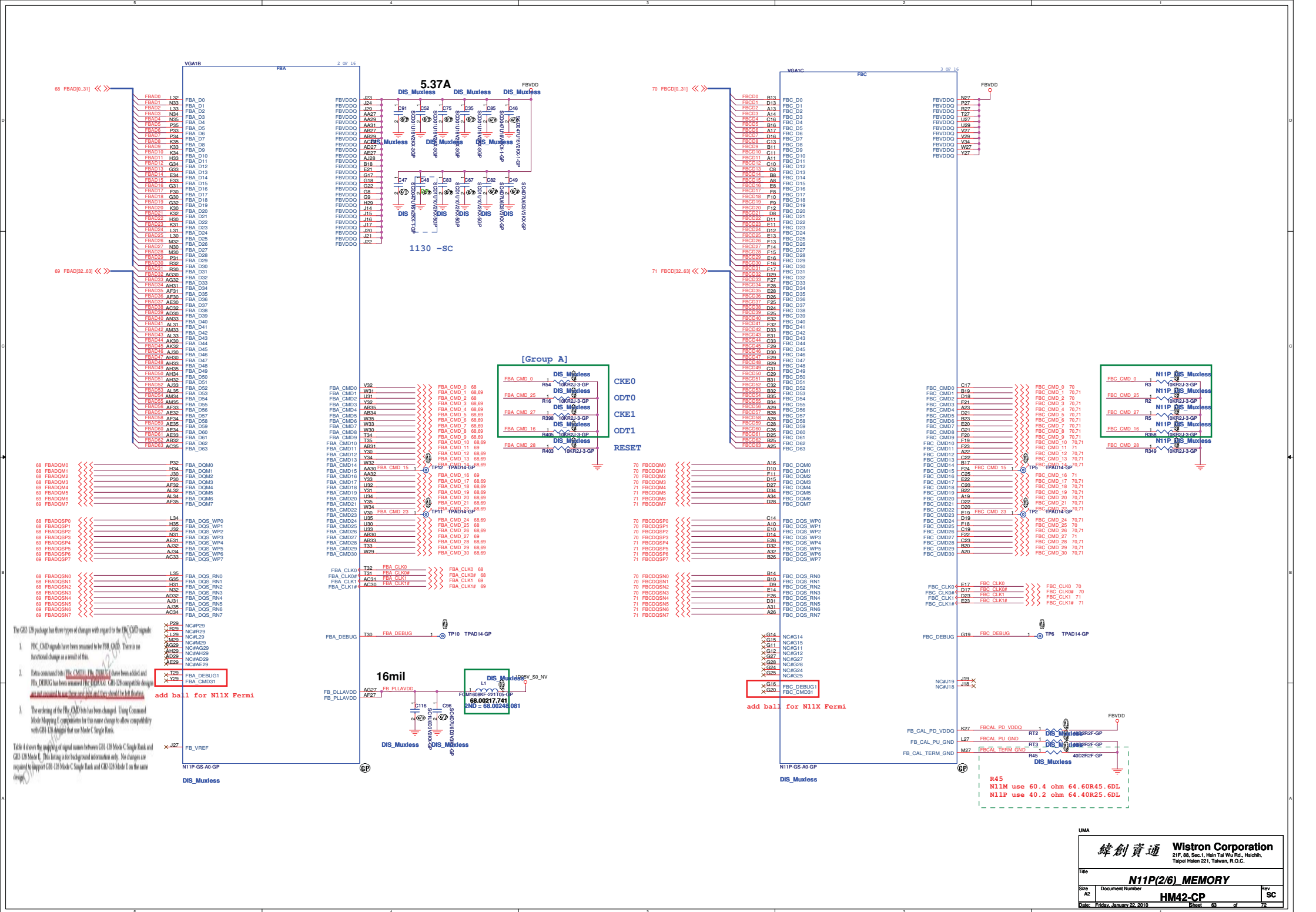
**Date: Friday, January 22, 2010**

**Sheet 61 of 72**

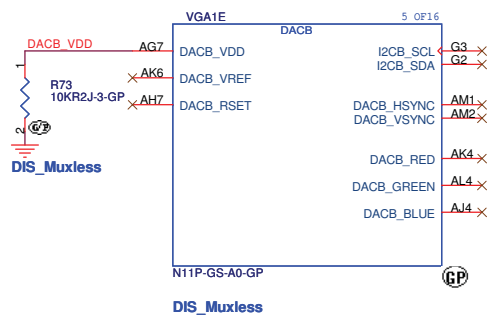
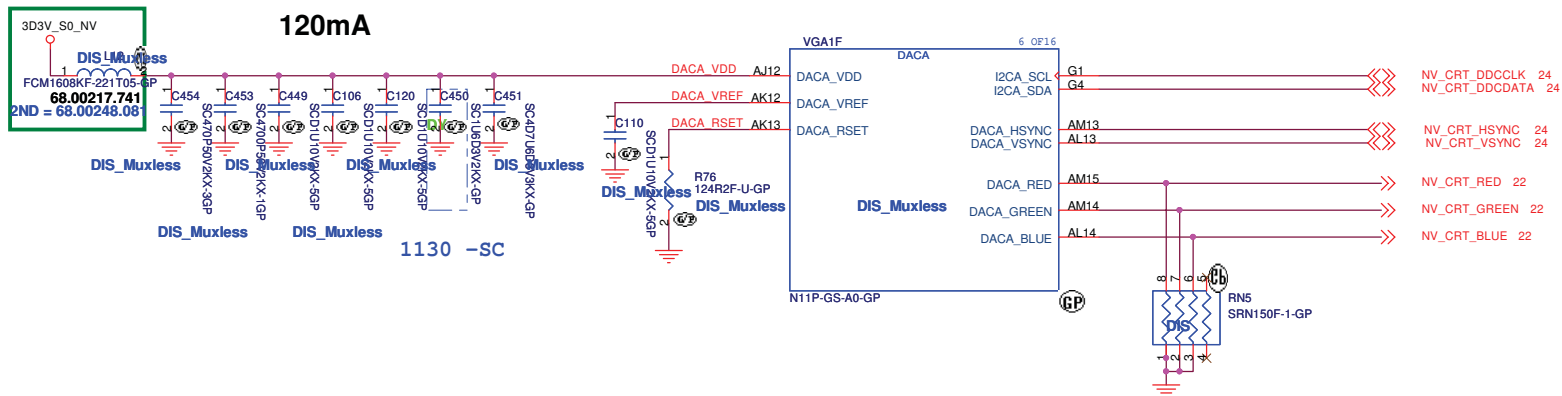






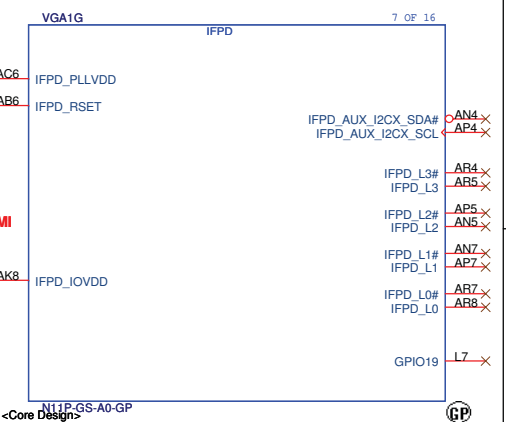
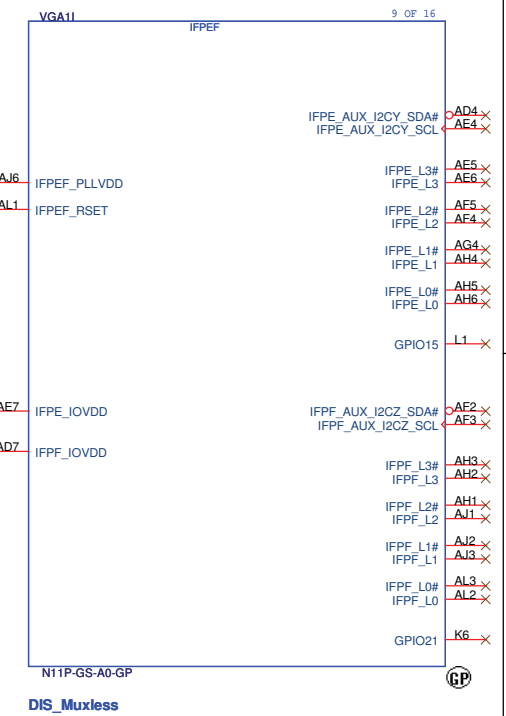
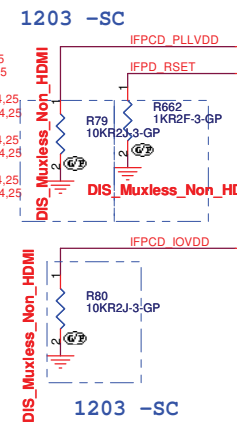
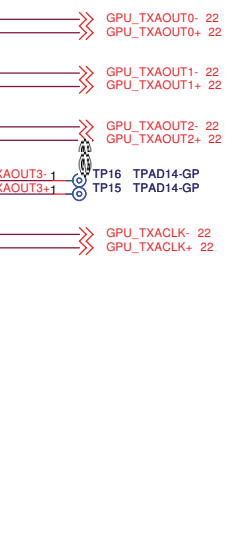
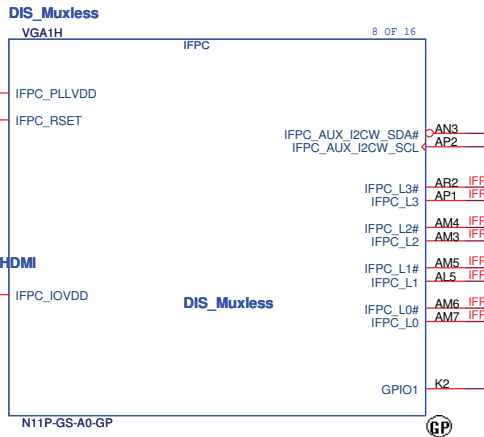
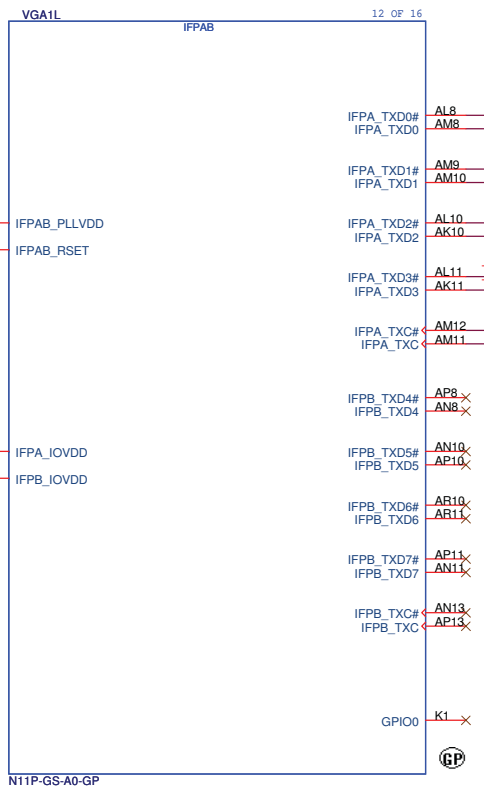
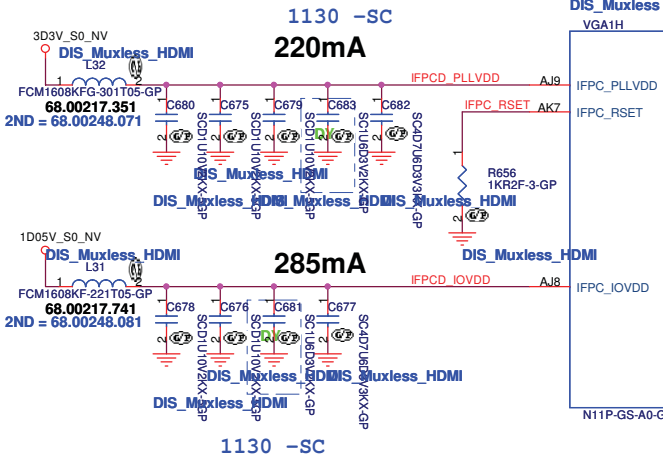
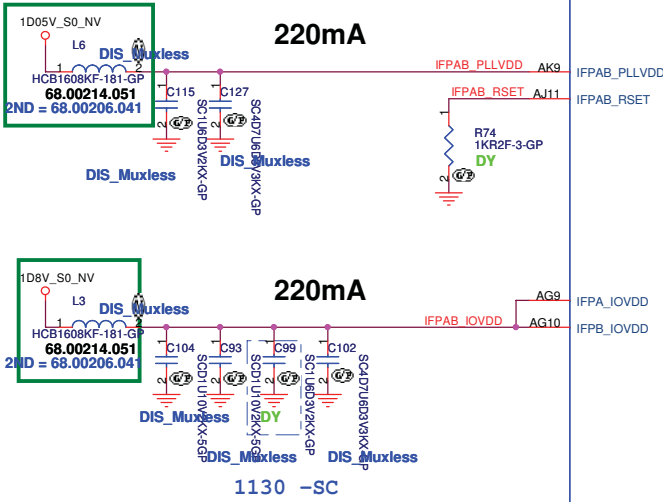




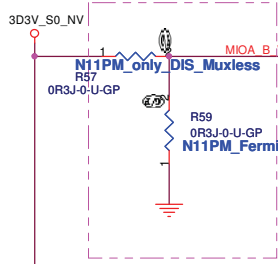


Discrete N11M

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>N11P(3/6) DAC</b>			
Size A3	Document Number		Rev SC
<b>HM42-CP</b>			
Date: Friday, January 22, 2010		Sheet 64 of 72	



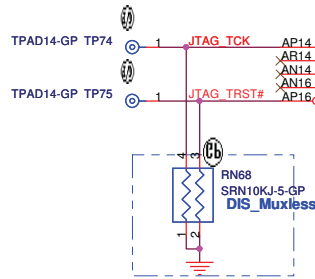
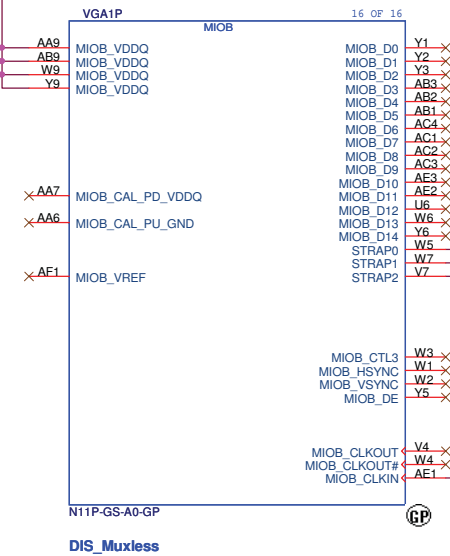
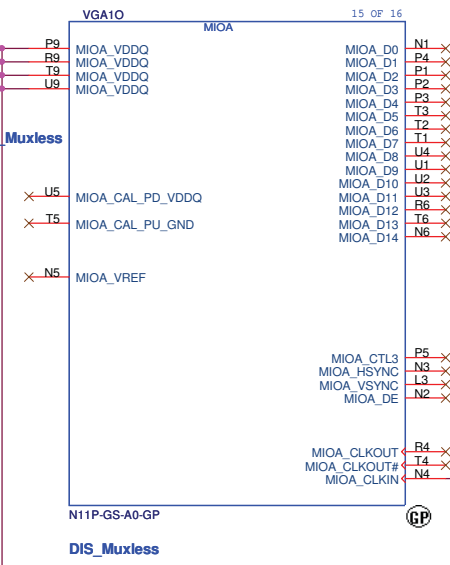
120mA



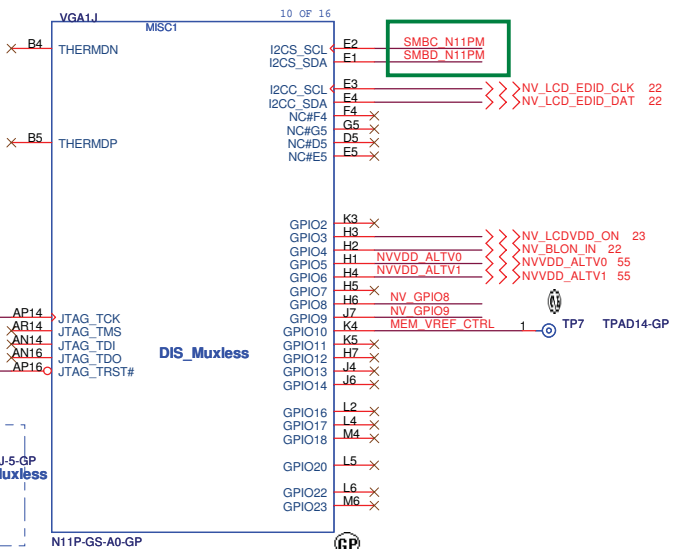
1006 -SA

N11P or N11M VGA stuff R277  
N11P or N11M Fermi VGA stuff R282

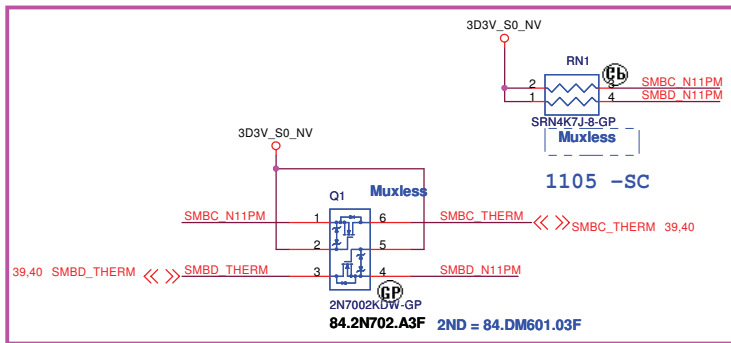
120mA



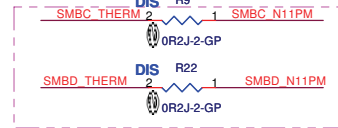
1202 -SC



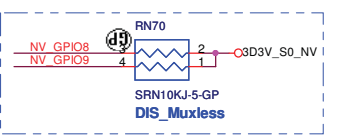
HM42-CP NV Muxless SA 0916



1105 -SC



HM42-CP NV Muxless SA 0923



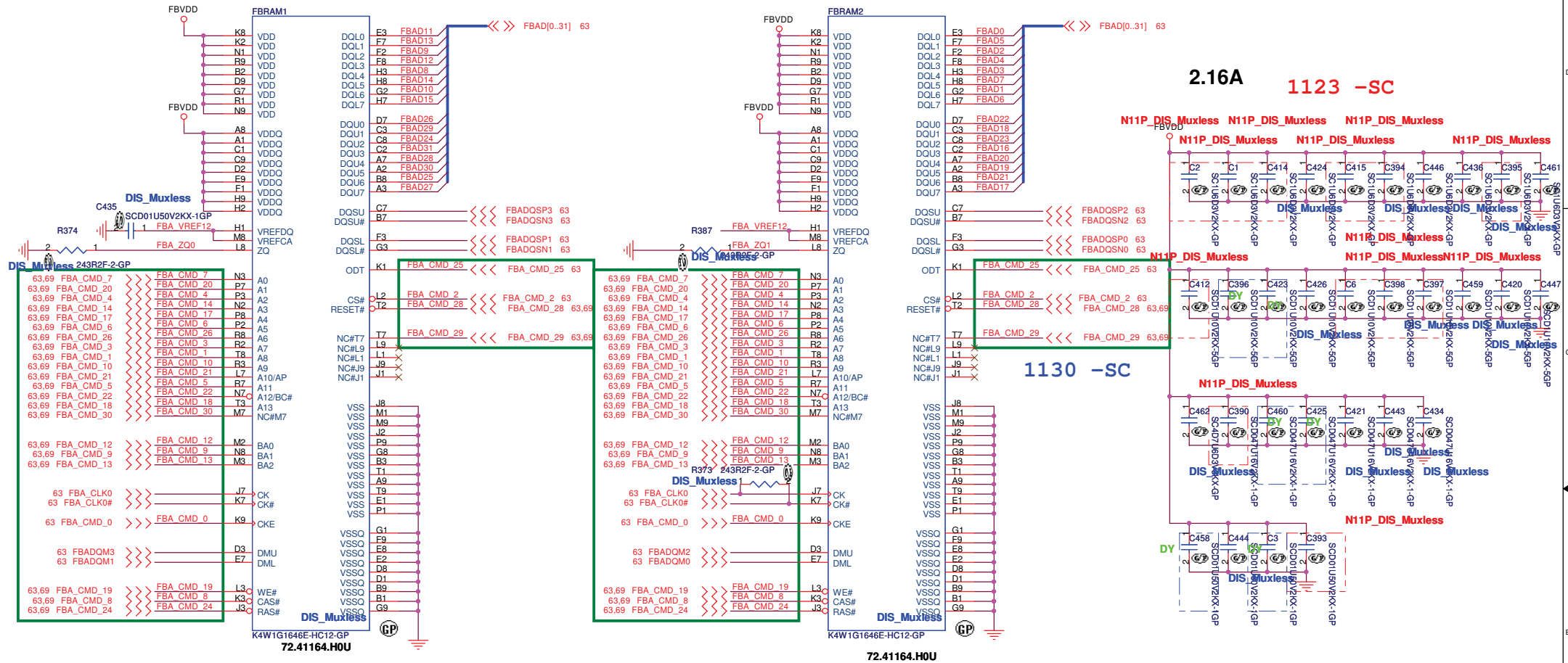
1202 -SC



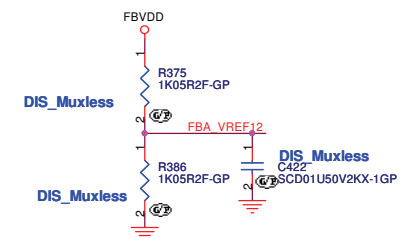
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
<b>N11P(6/6) POWER</b>			
Size A3	Document Number		Rev
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Date:	Friday, January 22, 2010	Sheet 67 of 72	

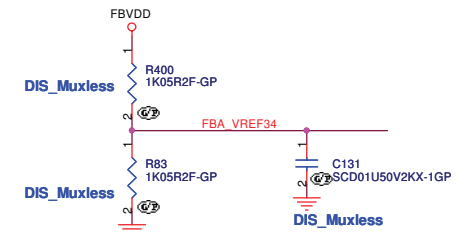
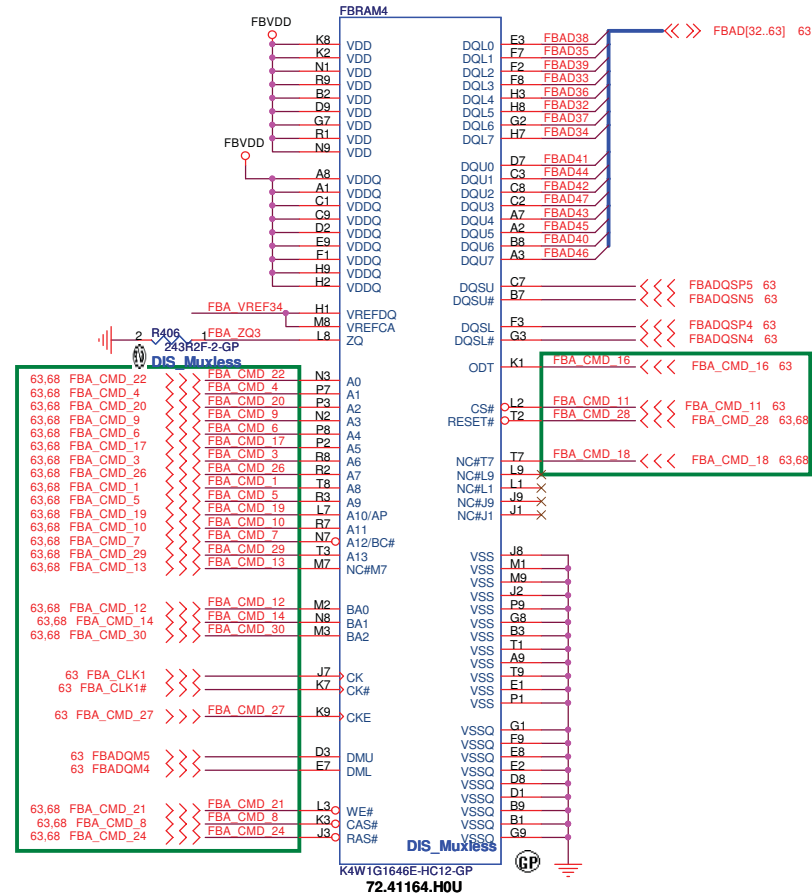
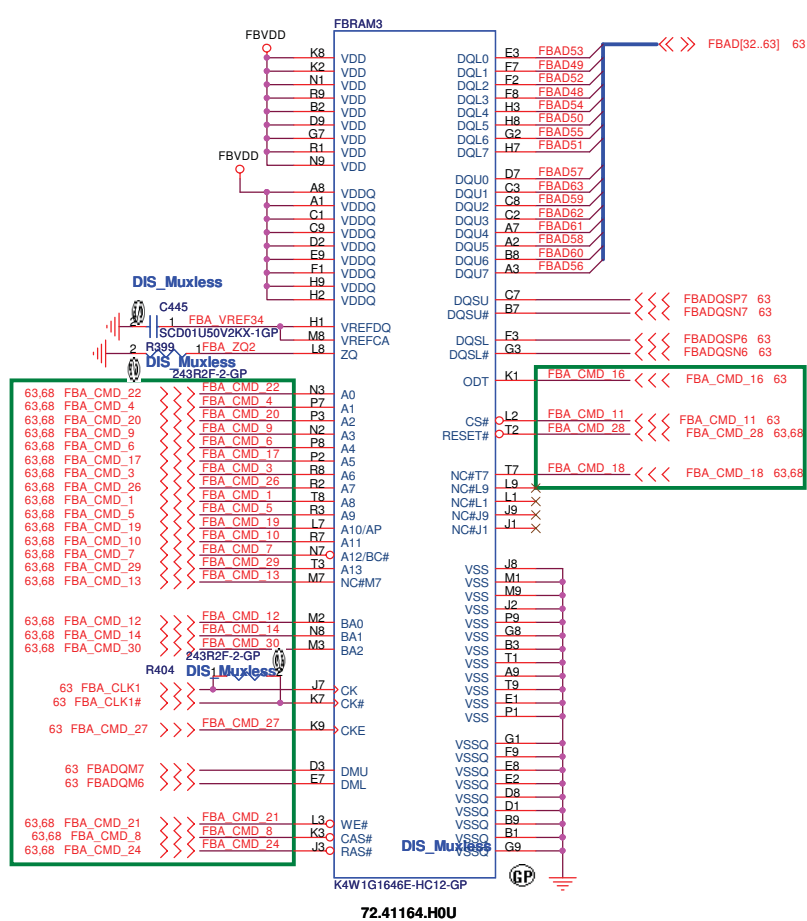
# DDR3



SAMSUNG: 72.41164.H0U(Use OEM PN:VR.1GB0B.006)  
HYNIX: 72.51G63.C0U(Use OEM PN: VR.1GB0G.004)



# DDR3

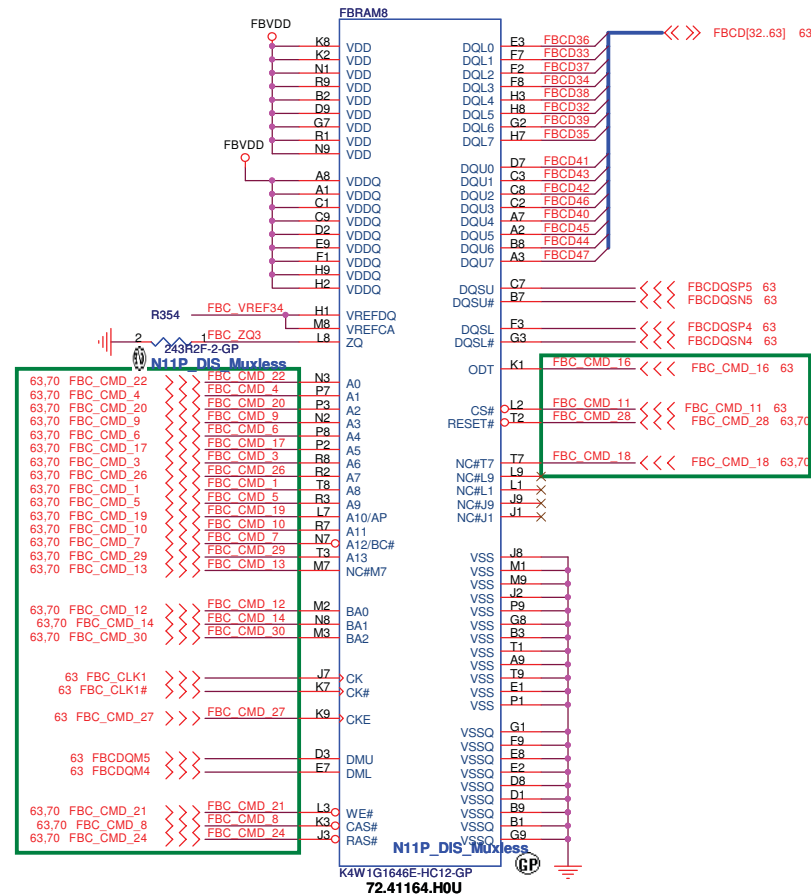
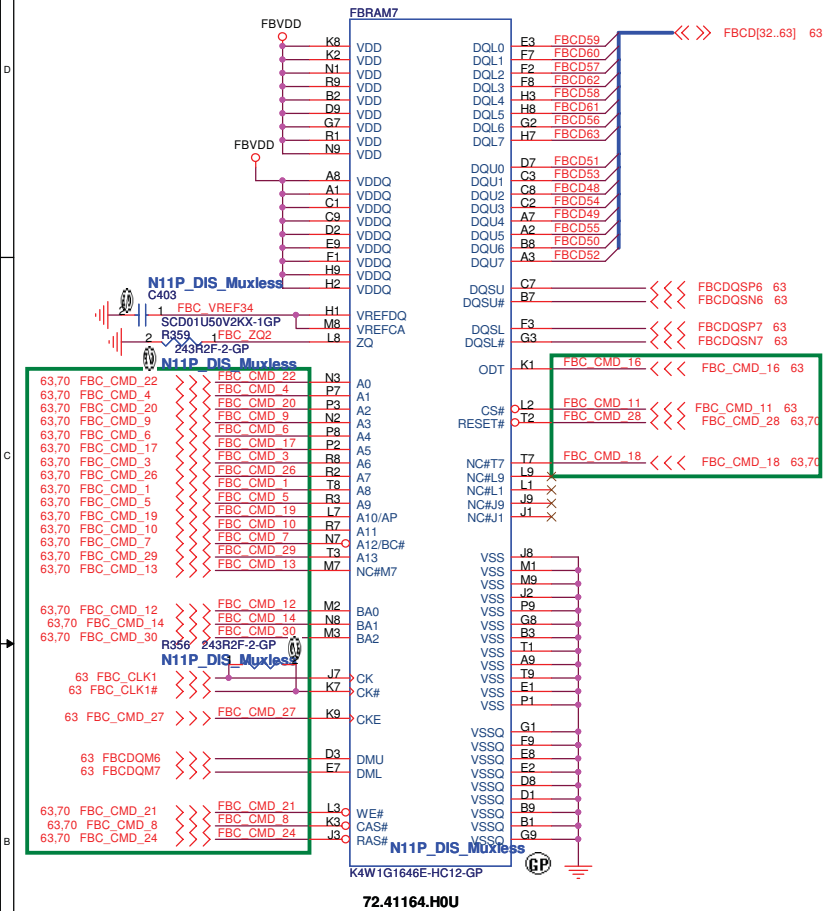


SAMSUNG: 72.41164.H0U  
HYNIX: 72.51G63.C0U



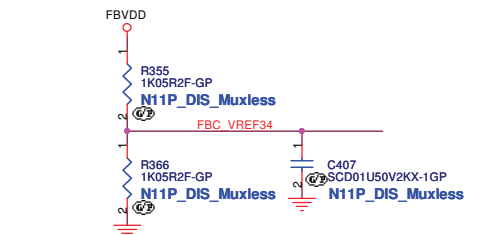


# DDR3



**SAMSUNG: 72.41164.H0U**

HYNIX: 72.51G63.C0U



UMA

**緯創資通** **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

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VRAM(4/4)			
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3) Samsung VRAM FBRAM1~8 PN:VR.1GB0B.006

Hynix VRAM FBRAM1~8 PN:VR.1GB0G.004

4) VGA 1 N11P-GE1 A3->71.0N11P.G0U,  
N11M-GE1-B -A3 -> 71.0N11M.E0U  
N11M-OP1 ->

6) VGA 1 N11P-GE1-> R53 49.9K(64.49925.6DL)  
N11M-GE1 -> R53 32.4K(64.32425.6DL)

7) R26 stuff Hynix VRAM : 15K(64.15025.6DL)  
Samsung VRAM : 20K(64.20025.6DL)

8) R45 stuff N11M use 60.4 ohm (64.32425.6DL)  
N11P use 40.2 ohm (64.40R25.6DL)

9) Muxless SKU stuff R181 2.37K (64.23715.6DL)  
UMA SKU Stuff R181 2.4K (64.24015.6DL)

10) N11M OP1 ->R392 15K(64.15025.6DL)  
N11M GE1 ->R392 30K(64.30025.6DL)

Mini Card 2nd and 3rd source PN confirm

Card Reader 2nd source confrim

## [ ECR ]

Date	released by	ECR Number
11/22	Anita	R1001240

[Old]

PCH1 PN : 71.0IBEX.A0U

[New]

PCH1 PN : 71.0HM55.00U(KI.G5501.002)

[lab -SB]

2nd -> UMA (S01G)

1st -> Diserete N11P Hynix(S02G)

1st +3rd -> Diserete N11M Hynix(S03G)

2nd +4th -> Diserete N11M Samsung(S04G)

1st -> Diserete N11P Samsung (S05G)

2nd -> N11M Hynix\_support Optimus (S06G)

[Eng -SC]

2nd -> UMA Non 3G (55.4GY01.S07G)

1st -> Diserete N11P Hynix\_3G(55.4GZ01.S03G)

1st +3rd -> Diserete N11M Hynix\_3G(55.4GY01.S09G)

2nd +4th -> Diserete N11M Samsung\_Non 3G(55.4GZ01.S02G)

1st + 5th -> Diserete N11P Samsung \_3G(55.4GY01.S10G)

1st +3 rd -> UMA Non 3G Non HDMI (55.4GW01.S01G)

[PD -1]

UMA 3G (55.4GY01.M01G)

Diserete N11P Hynix\_3G(55.4GY01.M02G) => 1st

Diserete N11P Hynix\_Non 3G(55.4GY01.M03G) => 2nd

UMA Non 3G (55.4GY01.M04G)

Diserete N11M Hynix\_3G(55.4GY01.M05G)

Diserete N11P Samsung \_3G(55.4GY01.M06G) =>1 st

Diserete N11M Samsung\_Non 3G(55.4GY01.M07G)

[PD action]

qual TPCN1 2nd source(20.K0296.006)

qual KB1 2nd source(20.K0382.026)

qual HDMI 2nd and 3rd

qual ODD1 3rd source(62.10065.E01)

qual PWRCN1 2nd and 3rd

qual RTC1 4th source

qual BT1 2nd and 3 source

qual U51 and U15 2nd source

qual TC13 2nd source(77.21571.111)

qual U32 2nd source

Qual HS1,HS2 2nd: 34.4B417.401

UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Modify History

Size

Document Number

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